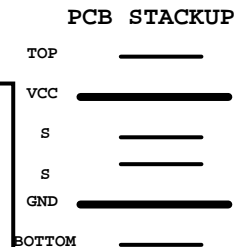


Project code: 91.4Z401.001
PCB P/N : 48.4Z401.011
REVISION : 07245-1



<Core Design>			
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Title			
BLOCK DIAGRAM			
Size A3	Document Number	Homa	Rev -1
Date:	Wednesday, March 19, 2008	Sheet 1 of	57

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config 1 bit 0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved, Rising Edge of PWROK.	This signal has a weak internal pull-down. This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	Tying this strap low configures DMI for ESI-compatible operation. This signal has a weak internal pull up. ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h: bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing. It has a weak internal pull up.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

PCI Routing

page 31

	IDSEL	INT	REQ	GNT
RTS5158	AD25	G: CARDBUS	0	0

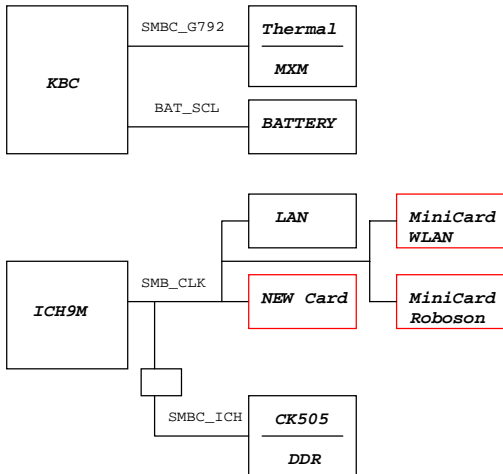
PCIe Routing

LANE1	LAN BCM5764MKMLG
LANE2	MiniCard WLAN
LANE3	MiniCard Roboson
LANE4	NewCard

SMBus

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	DOCK USB
4	USB3
5	Bluetooth
6	FP
7	MINIC1
8	WEBCAM
9	NEW1
10	MINIC2
11	NC



ICH9M Integrated Pull-up and Pull-down Resistors

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SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native CFG9 GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LAD[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1066 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG12	ALLZ	0 = ALLZ mode enabled (Note 3) 1 = Disabled (default)
CFG13	XOR	0 = XOR mode enabled (Note 3) 1 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH -> ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH -> ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIe disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

3. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

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Reference	
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6 H_A#(35..3) <<< H_A#(35..3)

U29A 1 OF 4

H_A#3 J4 A3#
H_A#4 L5 A4#
H_A#5 L4 A5#
H_A#6 M3 A6#
H_A#7 N2 A7#
H_A#8 N2 A8#
H_A#9 J1 A9#
H_A#10 N3 A10#
H_A#11 P5 A11#
H_A#12 L2 A12#
H_A#13 L2 A13#
H_A#14 P4 A14#
H_A#15 P1 A15#
H_A#16 R1 A16#

6 H_ADSTB#0 <<< H_REQ#(4..0) <<< H_REQ#(4..0)

H_REQ#0 K3 REQ#0
H_REQ#1 H2 REQ#1
H_REQ#2 K2 REQ#2
H_REQ#3 J3 REQ#3
H_REQ#4 L1 REQ#4

H_A#17 Y2 A17#
H_A#18 U6 A18#
H_A#19 R3 A19#
H_A#20 W6 A20#
H_A#21 U4 A21#
H_A#22 Y5 A22#
H_A#23 U1 A23#
H_A#24 R4 A24#
H_A#25 T3 A25#
H_A#26 T3 A26#
H_A#27 W2 A27#
H_A#28 W5 A28#
H_A#29 Y4 A29#
H_A#30 U2 A30#
H_A#31 V4 A31#
H_A#32 W3 A32#
H_A#33 AA4 A33#
H_A#34 AB2 A34#
H_A#35 AA3 A35#

6 H_ADSTB#1 <<< H_A20M# <<< H_FERR# <<< H_IGNNE#

H_A20M# A6 A20M#
H_FERR# A5 FERR#
H_IGNNE# C4 IGNNE#

21 H_STPCLK# <<< R100 2H_STPCLK# <<< H_INTR# <<< H_NMI# <<< H_SMI#

STPCLK# D5
LINT0 C6
LINT1 B4
SMI# A3

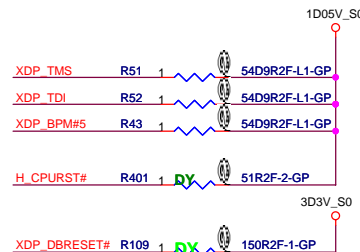
RESERVED
RSVD#M4 M4
RSVD#N5 N5
RSVD#T2 T2
RSVD#V3 V3
RSVD#B2 B2
RSVD#C3 C3
RSVD#D2 D2
RSVD#D22 D22
RSVD#D3 D3
RSVD#F6 F6

KEY_NC B1

BGA479-SKT6-GPU6

62.10079.001

1ST = 62.10053.401



All place within 2" to CPU

Place testpoint on H_IERR# with a GND 0.1" away



CPU_PROCHOT# <<< H_THERMDA 25 <<< H_THERMDC 25

PM_THRMTRIP# <<< R104 2 <<< PM_THRMTRIP-A# 7,21,48

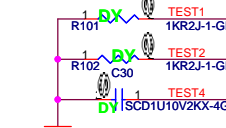
CLK_CPU_BCLK 3 <<< CLK_CPU_BCLK 3

Layout Note: "CPU_GTLREF0" 0.5" max length.



TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26

3.7 CPU_SEL0 <<< B22
3.7 CPU_SEL1 <<< B23
3.7 CPU_SEL2 <<< C21



Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

BGA479-SKT6-GPU6

1ST = 62.10053.401

U29B 2 OF 4

H_D#0 E22 D0#
H_D#1 E24 D1#
H_D#2 E26 D2#
H_D#3 G22 D3#
H_D#4 F23 D4#
H_D#5 G25 D5#
H_D#6 E25 D6#
H_D#7 E23 D7#
H_D#8 K24 D8#
H_D#9 G24 D9#
H_D#10 J24 D10#
H_D#11 J23 D11#
H_D#12 H22 D12#
H_D#13 F26 D13#
H_D#14 K22 D14#
H_D#15 H23 D15#

6 H_DSTBN#0 <<< DSTBN#0
6 H_DSTBP#0 <<< DSTBP#0
6 H_DINV#0 <<< DINV#0

H_D#16 N22 D16#
H_D#17 K25 D17#
H_D#18 P26 D18#
H_D#19 R23 D19#
H_D#20 L23 D20#
H_D#21 M24 D21#
H_D#22 L22 D22#
H_D#23 M23 D23#
H_D#24 P25 D24#
H_D#25 P23 D25#
H_D#26 P22 D26#
H_D#27 T24 D27#
H_D#28 R24 D28#
H_D#29 L25 D29#
H_D#30 T25 D30#
H_D#31 N25 D31#

6 H_DSTBN#1 <<< DSTBN#1
6 H_DSTBP#1 <<< DSTBP#1
6 H_DINV#1 <<< DINV#1

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

3.7 CPU_SEL0 <<< B22
3.7 CPU_SEL1 <<< B23
3.7 CPU_SEL2 <<< C21

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

H_DINV#(3..0) <<< H_DINV#(3..0) 6
H_DSTBN#(3..0) <<< H_DSTBN#(3..0) 6
H_DSTBP#(3..0) <<< H_DSTBP#(3..0) 6
H_D#(63..0) <<< H_D#(63..0) 6

H_D#32 Y22 H_D#32
H_D#33 AB24 H_D#33
H_D#34 V24 H_D#34
H_D#35 V26 H_D#35
H_D#36 V23 H_D#36
H_D#37 T22 H_D#37
H_D#38 U25 H_D#38
H_D#39 V25 H_D#39
H_D#40 W22 H_D#40
H_D#41 W24 H_D#41
H_D#42 W24 H_D#42
H_D#43 W24 H_D#43
H_D#44 W24 H_D#44
H_D#45 W24 H_D#45
H_D#46 W24 H_D#46
H_D#47 W24 H_D#47

6 H_DSTBN#2 <<< DSTBN#2 6
6 H_DSTBP#2 <<< DSTBP#2 6
6 H_DINV#2 <<< DINV#2 6

H_D#48 AE24 H_D#48
H_D#49 AD24 H_D#49
H_D#50 AA21 H_D#50
H_D#51 AB22 H_D#51
H_D#52 AC21 H_D#52
H_D#53 AC26 H_D#53
H_D#54 AD20 H_D#54
H_D#55 AE22 H_D#55
H_D#56 AE23 H_D#56
H_D#57 AC25 H_D#57
H_D#58 AE21 H_D#58
H_D#59 AD21 H_D#59
H_D#60 AC22 H_D#60
H_D#61 AD23 H_D#61
H_D#62 AE22 H_D#62
H_D#63 AC23 H_D#63

6 H_DSTBN#3 <<< DSTBN#3 6
6 H_DSTBP#3 <<< DSTBP#3 6
6 H_DINV#3 <<< DINV#3 6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

3.7 CPU_SEL0 <<< B22
3.7 CPU_SEL1 <<< B23
3.7 CPU_SEL2 <<< C21

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

TEST1 C23
TEST2 D25
TEST3 AF24
TEST4 AF26
TEST5 TEST5
TEST6 TEST6

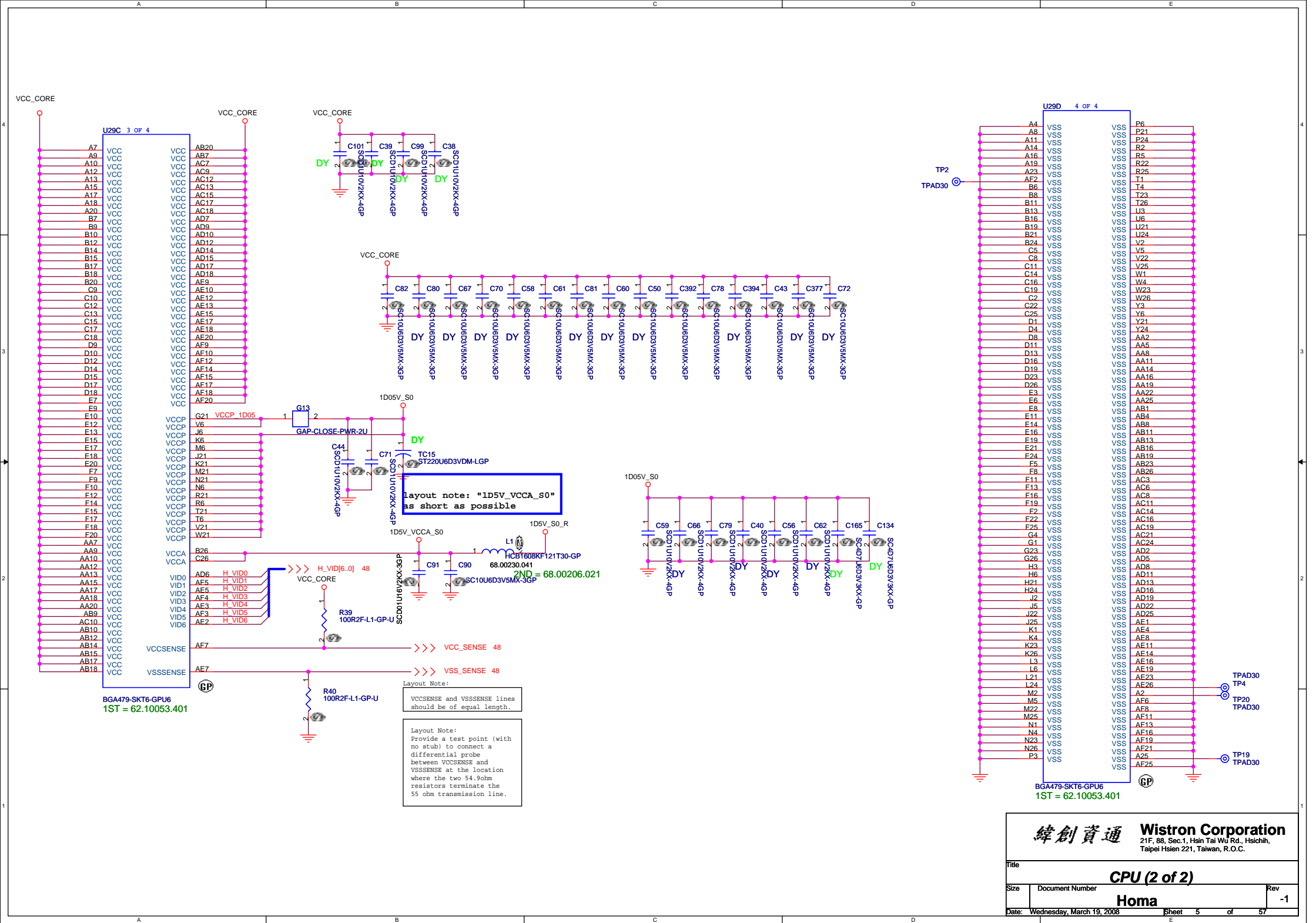
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TEST3 AF24
TEST4 AF26
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TEST6 TEST6

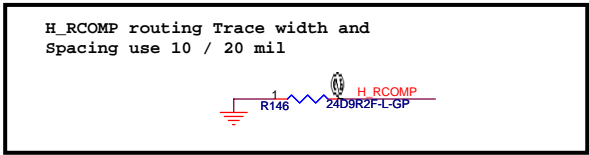
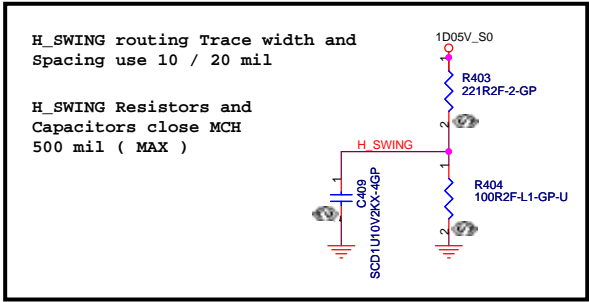
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TEST5 TEST5
TEST6 TEST6

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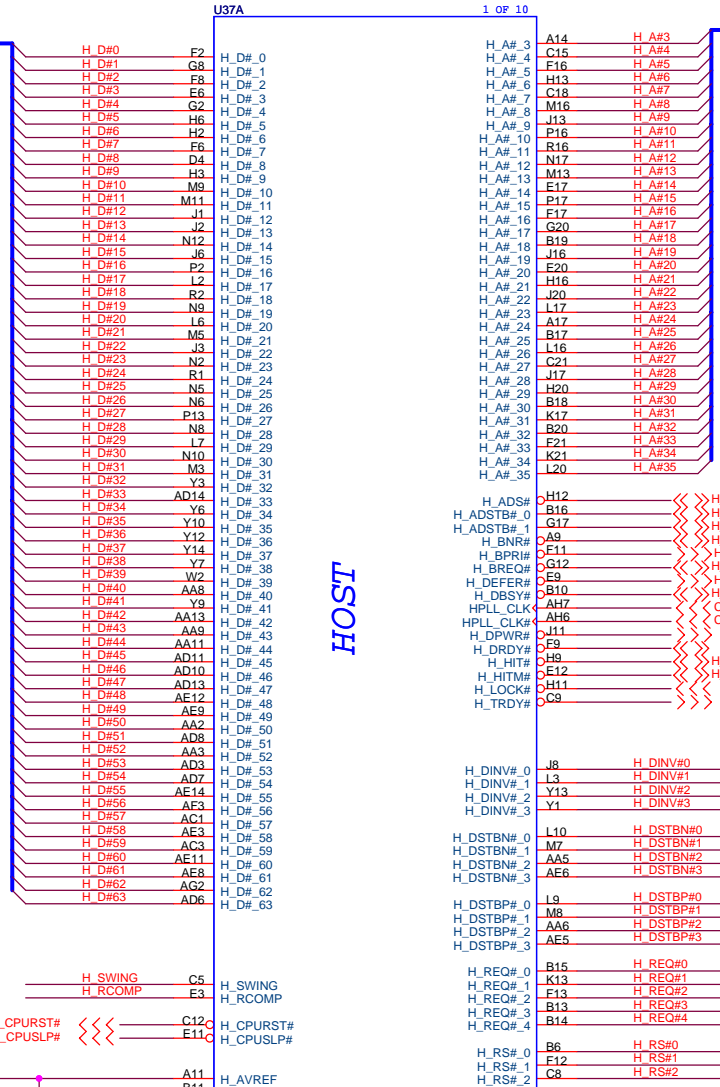
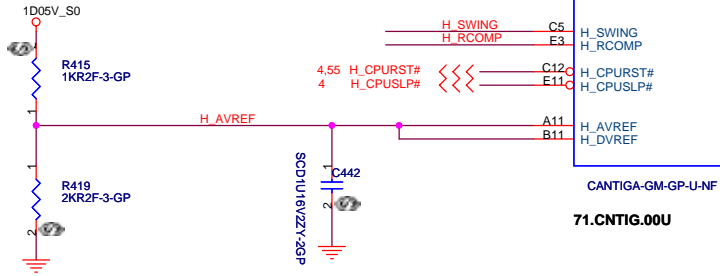
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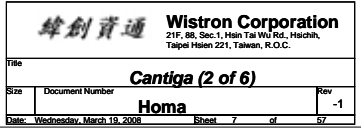
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Size Document Number
Date: Wednesday, March 19, 2008 Sheet 4 of 57
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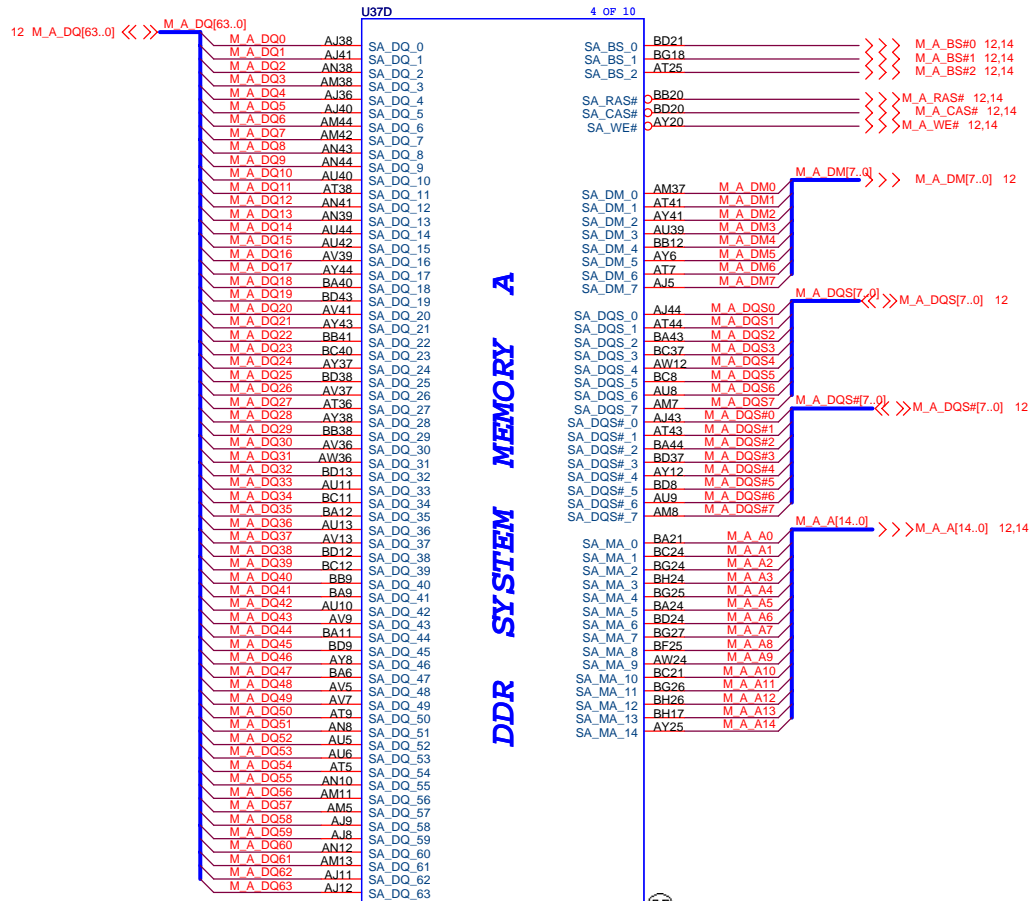




Place them near to the chip (< 0.5")

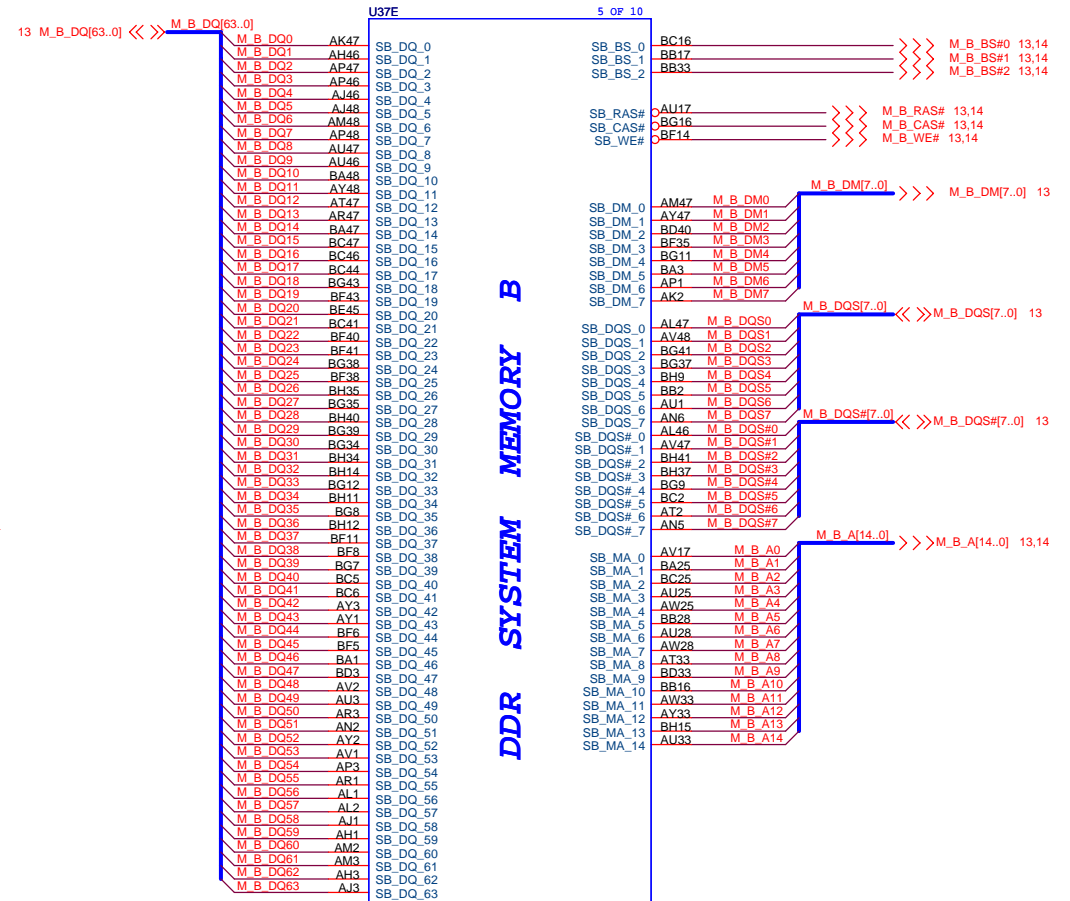






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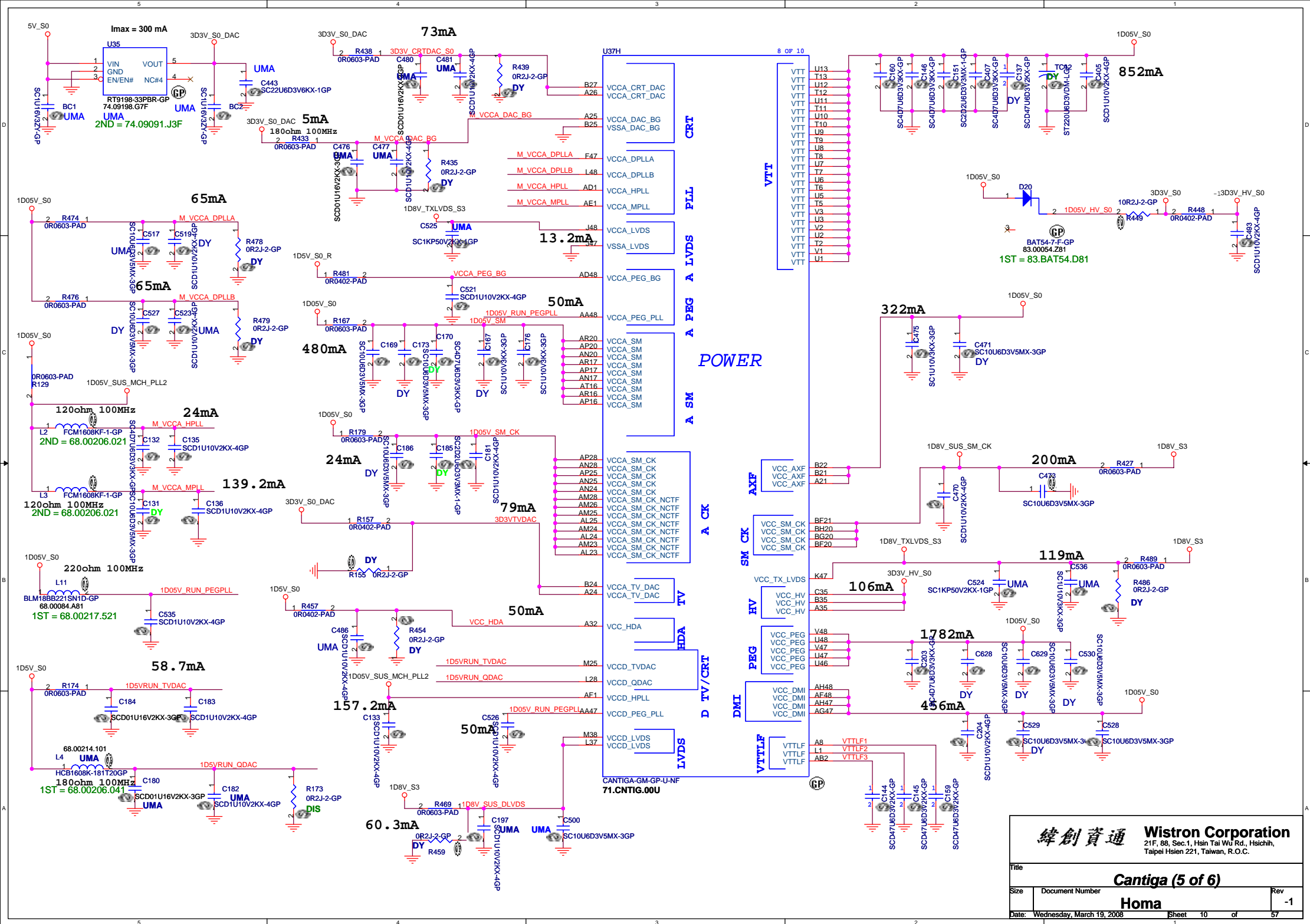
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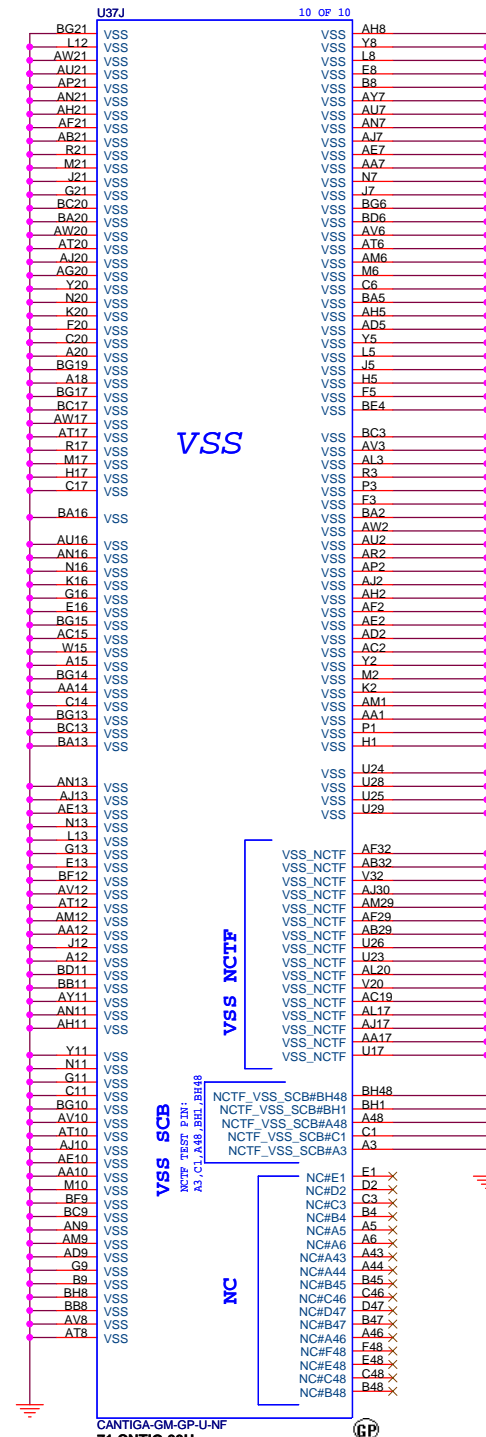
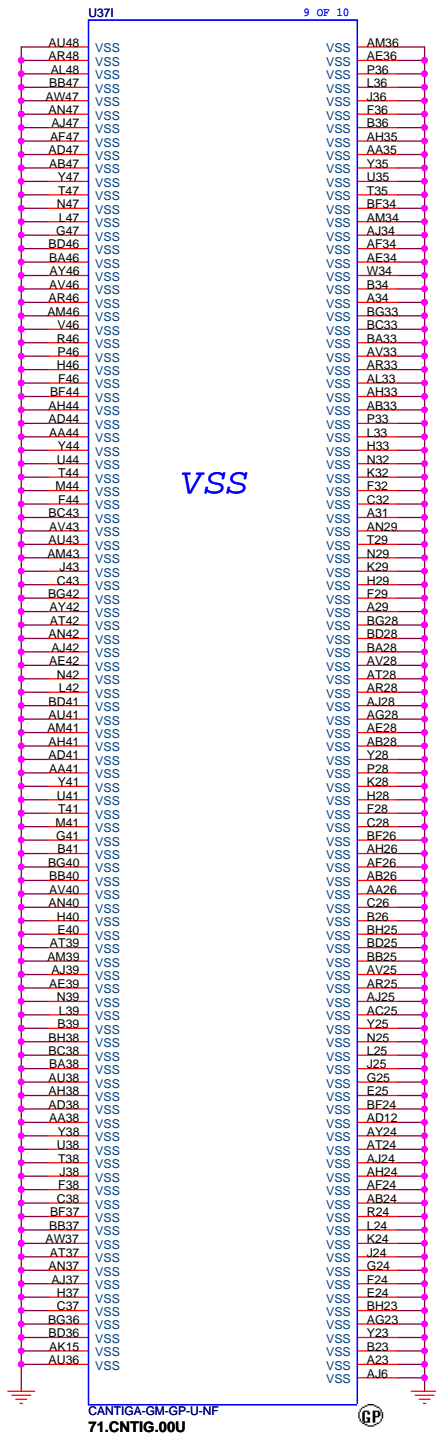


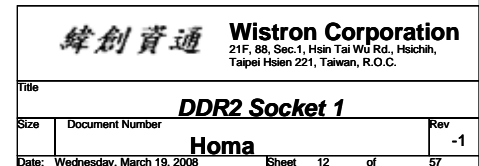
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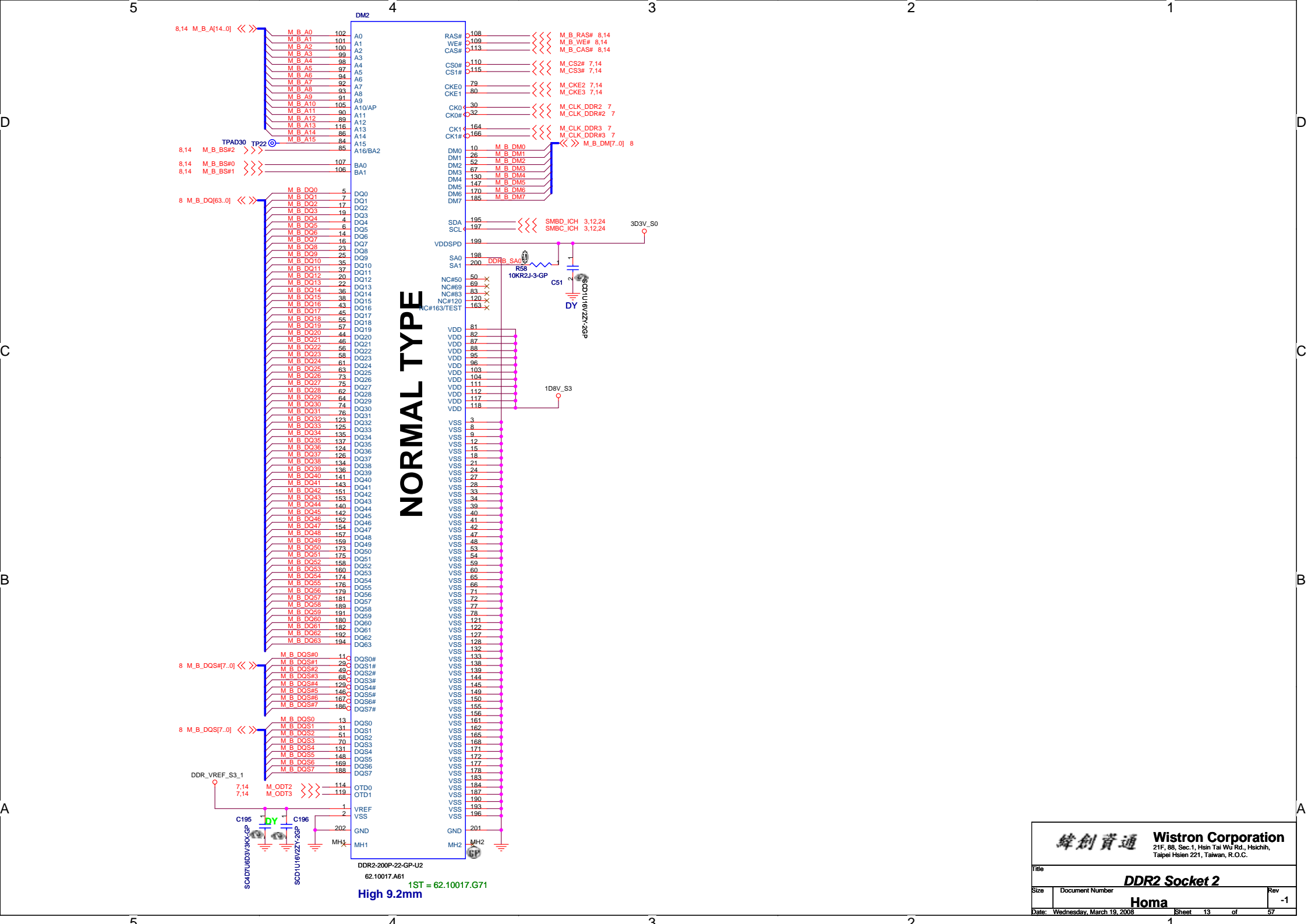
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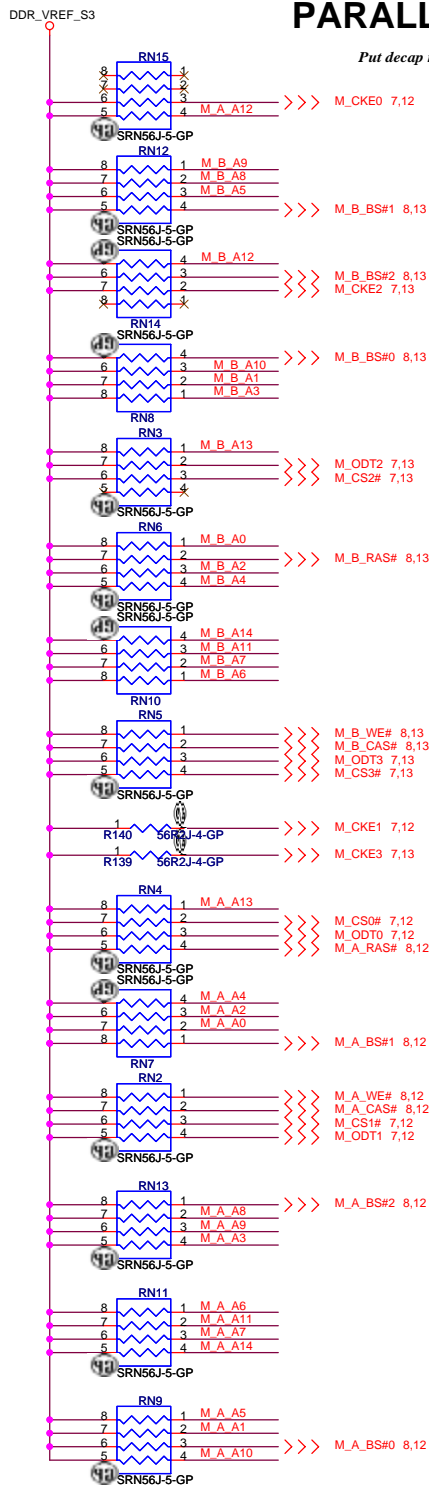






PARALLEL TERMINATION

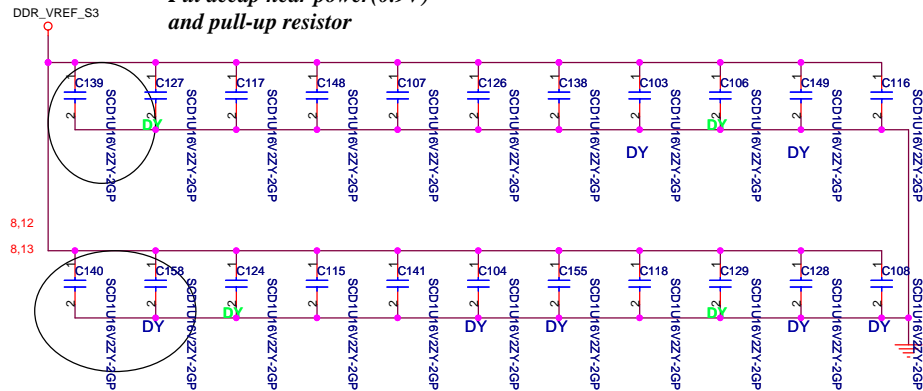
Put decap near power(0.9V) and pull-up resistor



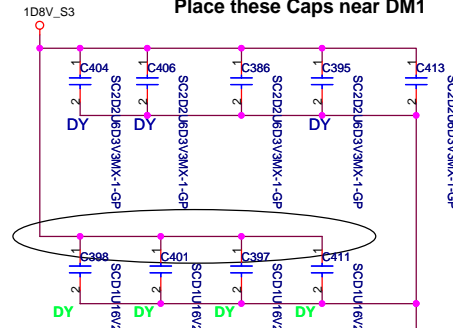
M_A_A[14..0] << M_A_A[14..0] 8,12
M_B_A[14..0] << M_B_A[14..0] 8,13

Decoupling Capacitor

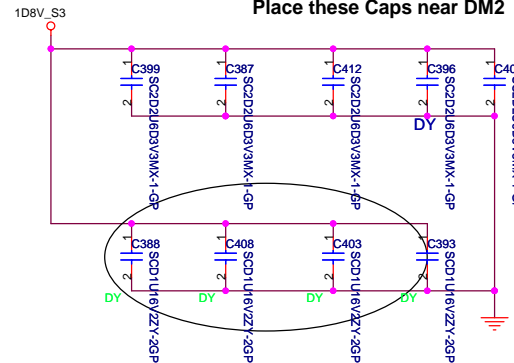
Put decap near power(0.9V) and pull-up resistor



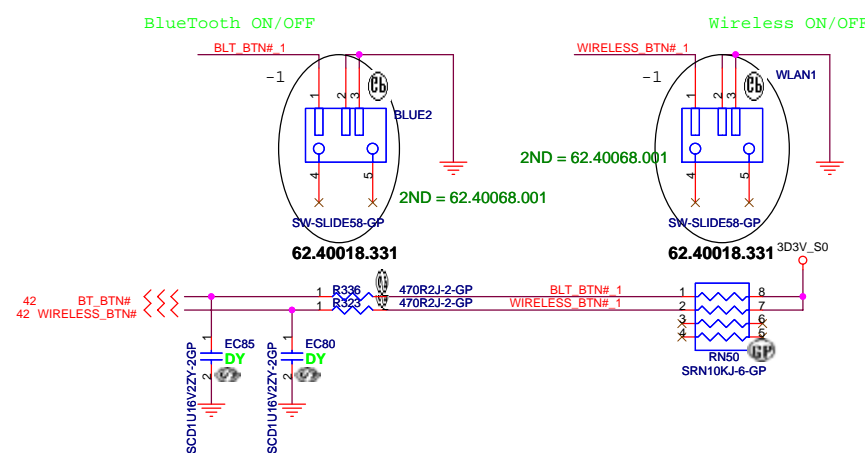
Place these Caps near DM1

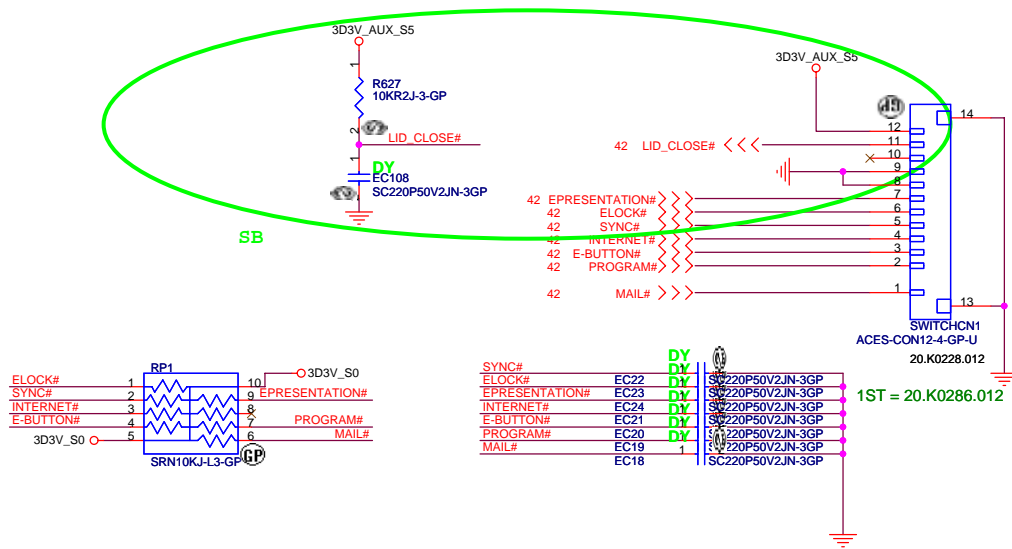


Place these Caps near DM2



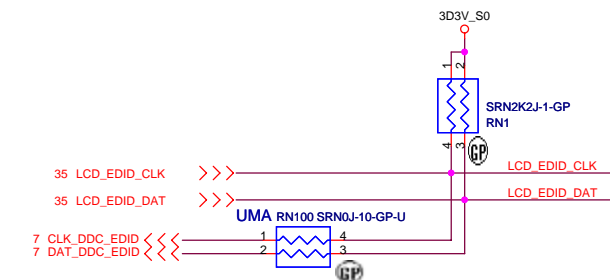
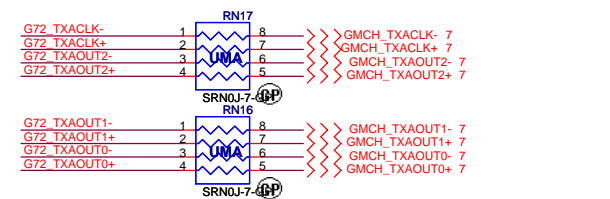
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3D3V_AUX_S5	1	TP119	TPAD34
LID_CLOSE#	1	TP121	TPAD34
SYNC#	1	TP120	TPAD34
ELOCK#	1	TP122	TPAD34
EPRESENTATION#	1	TP124	TPAD34
INTERNET#	1	TP123	TPAD34
E-BUTTON#	1	TP126	TPAD34
PROGRAM#	1	TP125	TPAD34
MAIL#	1	TP127	TPAD34

LCD/INVERTER/CCD CONN



<Core Design>

緯創資通

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Title

LCD CONN

Size

Document Number

Homa

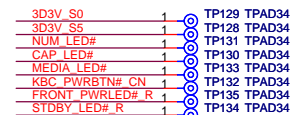
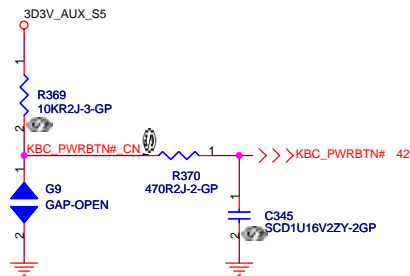
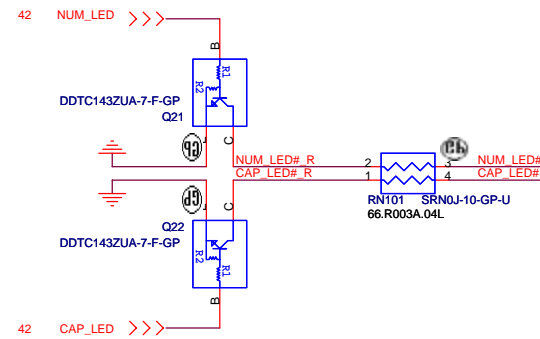
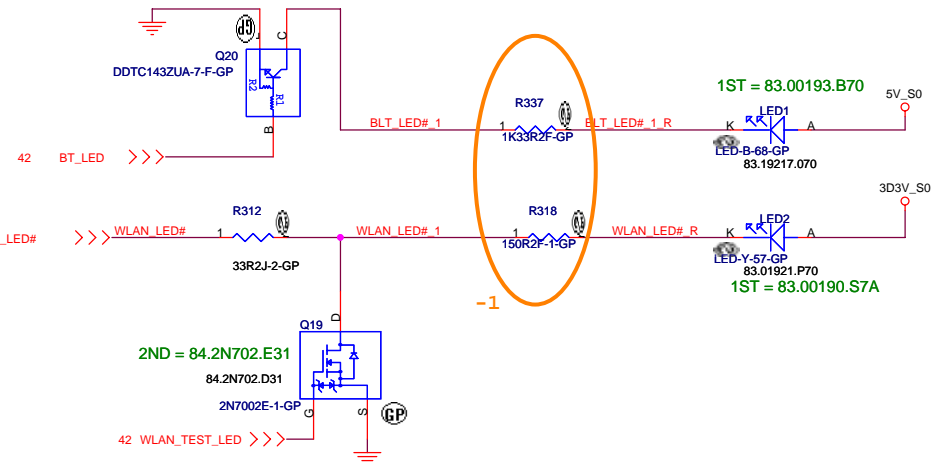
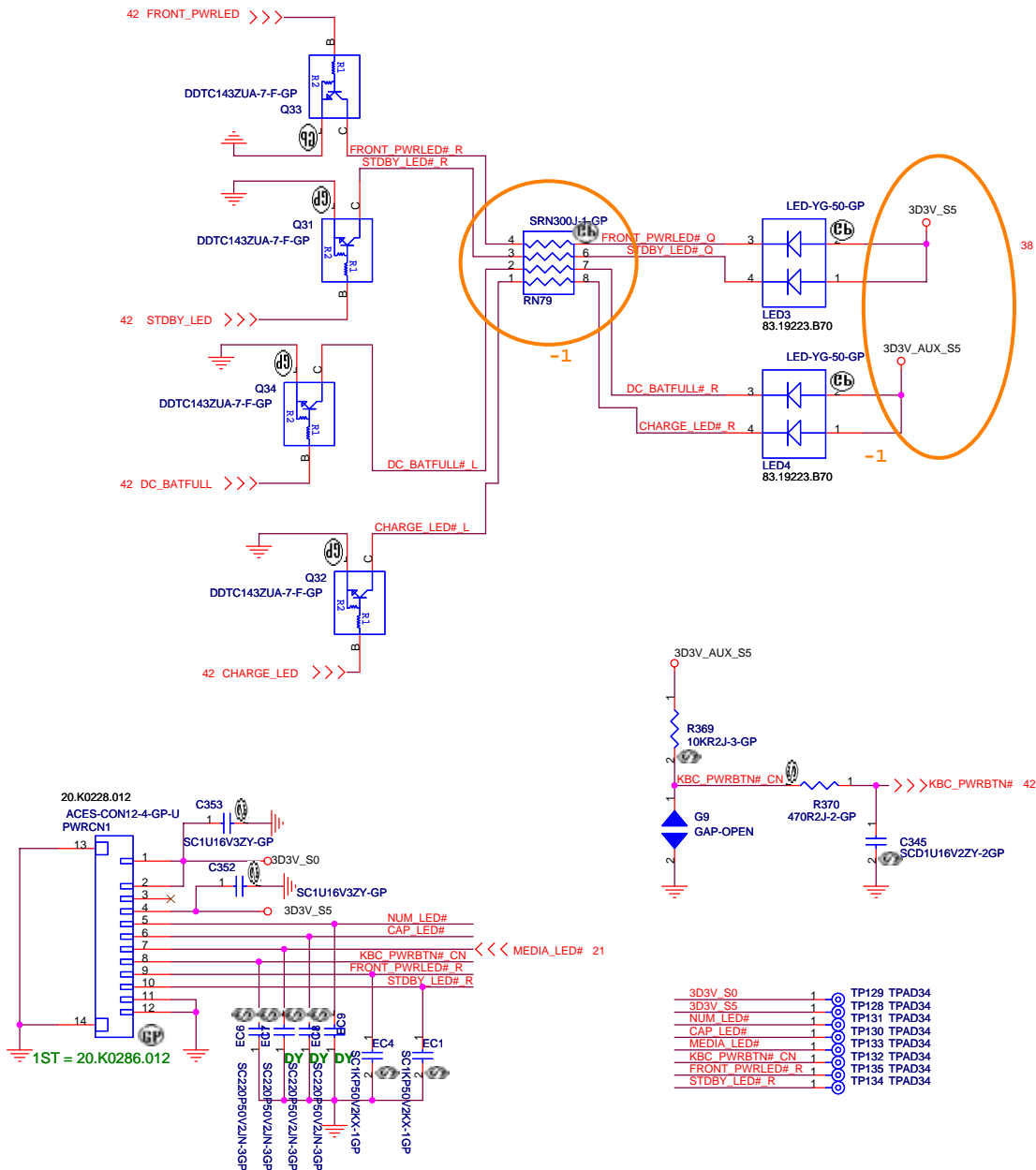
Date: Wednesday, March 19, 2008

Sheet 17

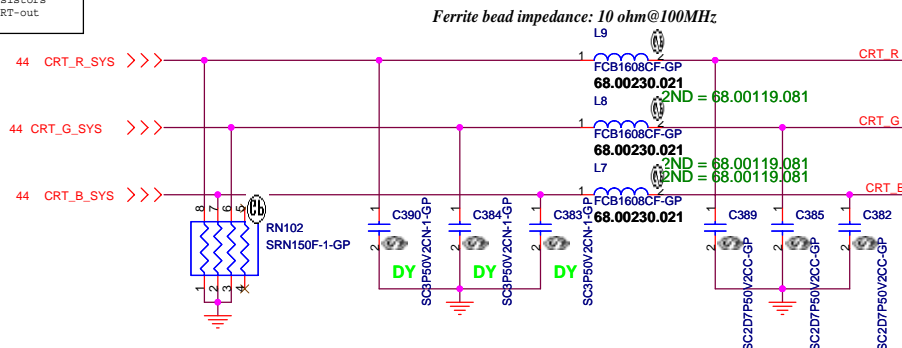
Rev

Rev
-1

LED

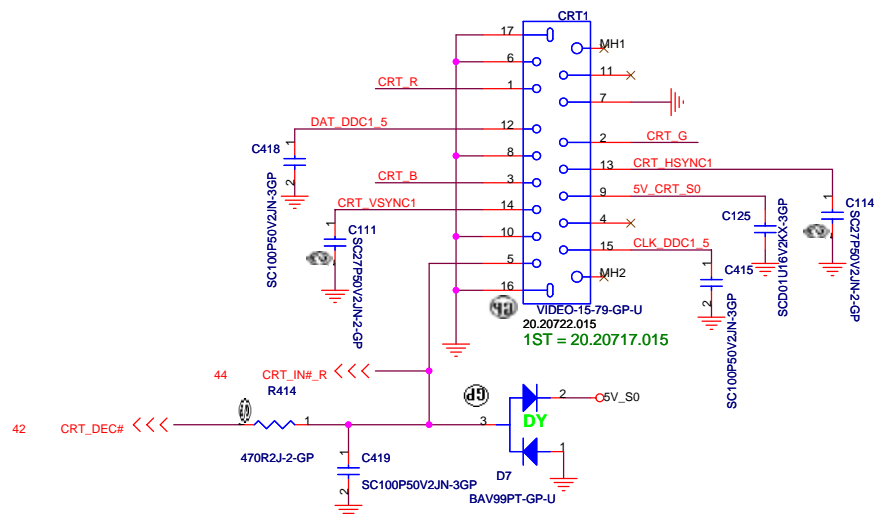


Layout Note:
Place these resistors
close to the CRT-out
connector

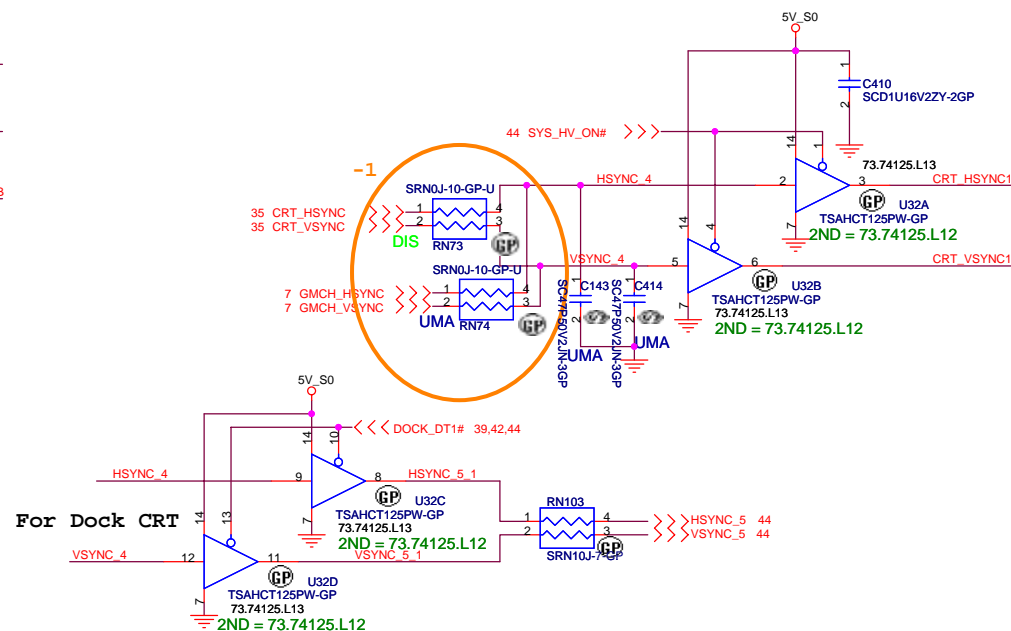


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

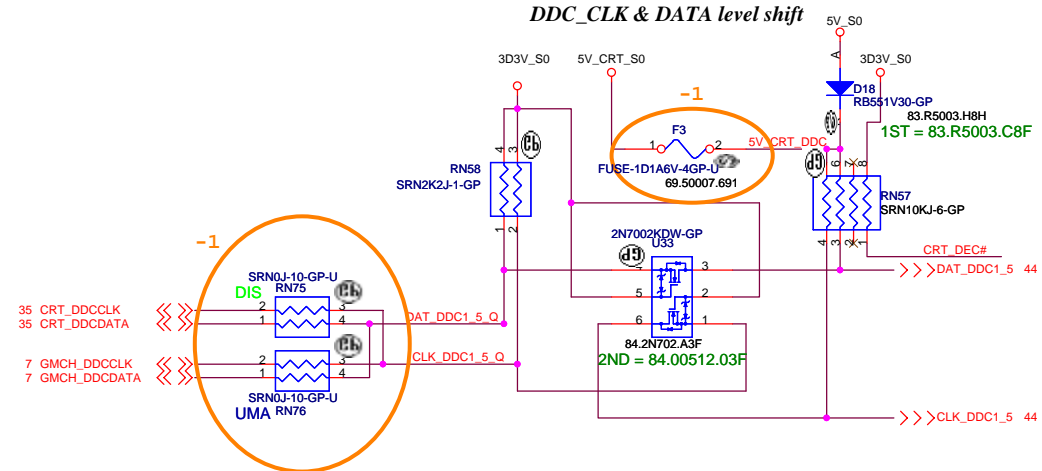
CRT I/F & CONNECTOR



Hsync & Vsync level shift



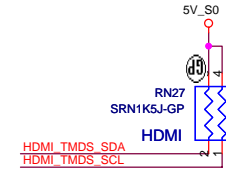
DDC_CLK & DATA level shift



<Core Design>

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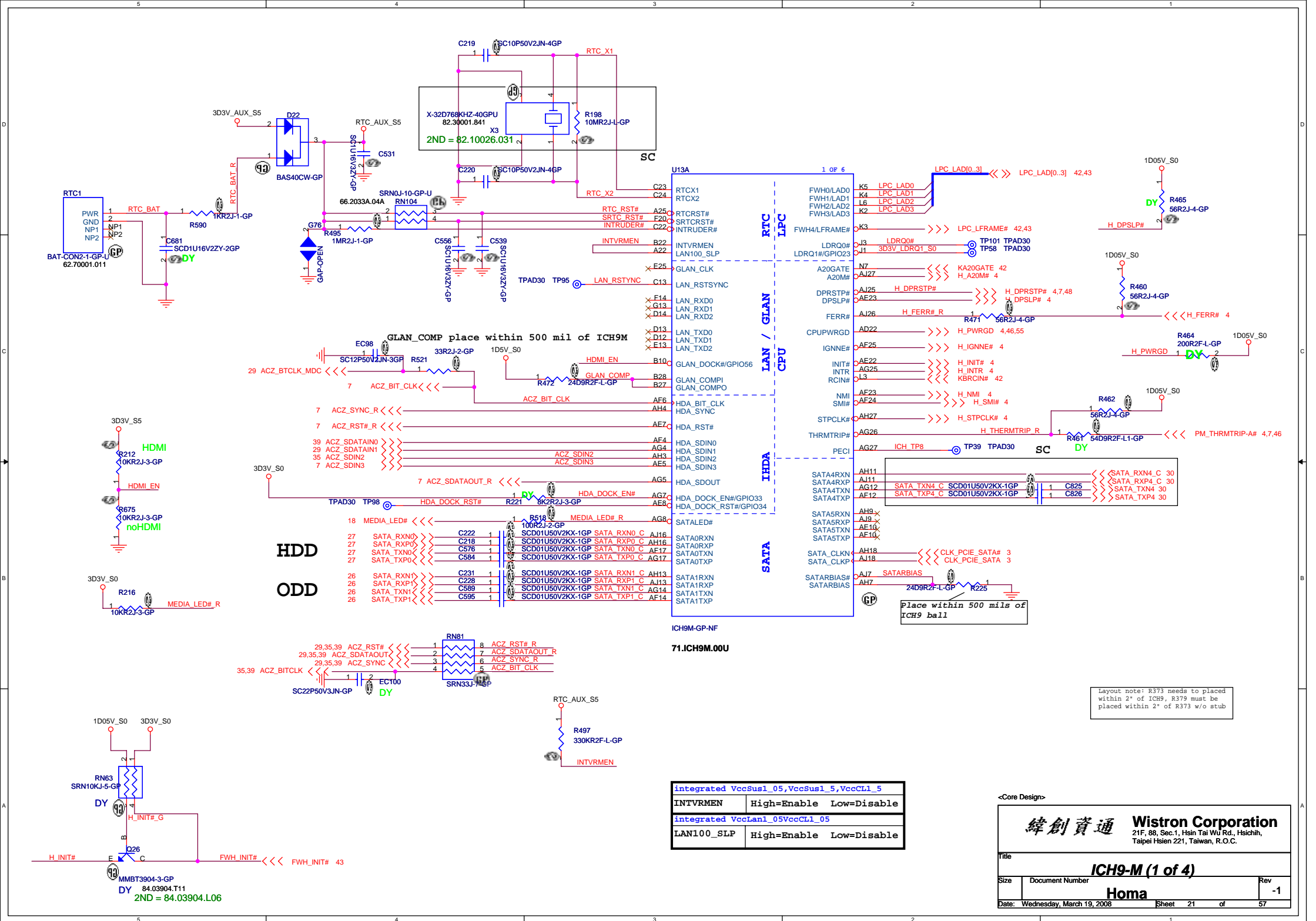
Title		
CRT Connector		
Size	Document Number	Rev
	Homa	-1
Date: Wednesday, March 19, 2008		
Sheet 19 of 57		

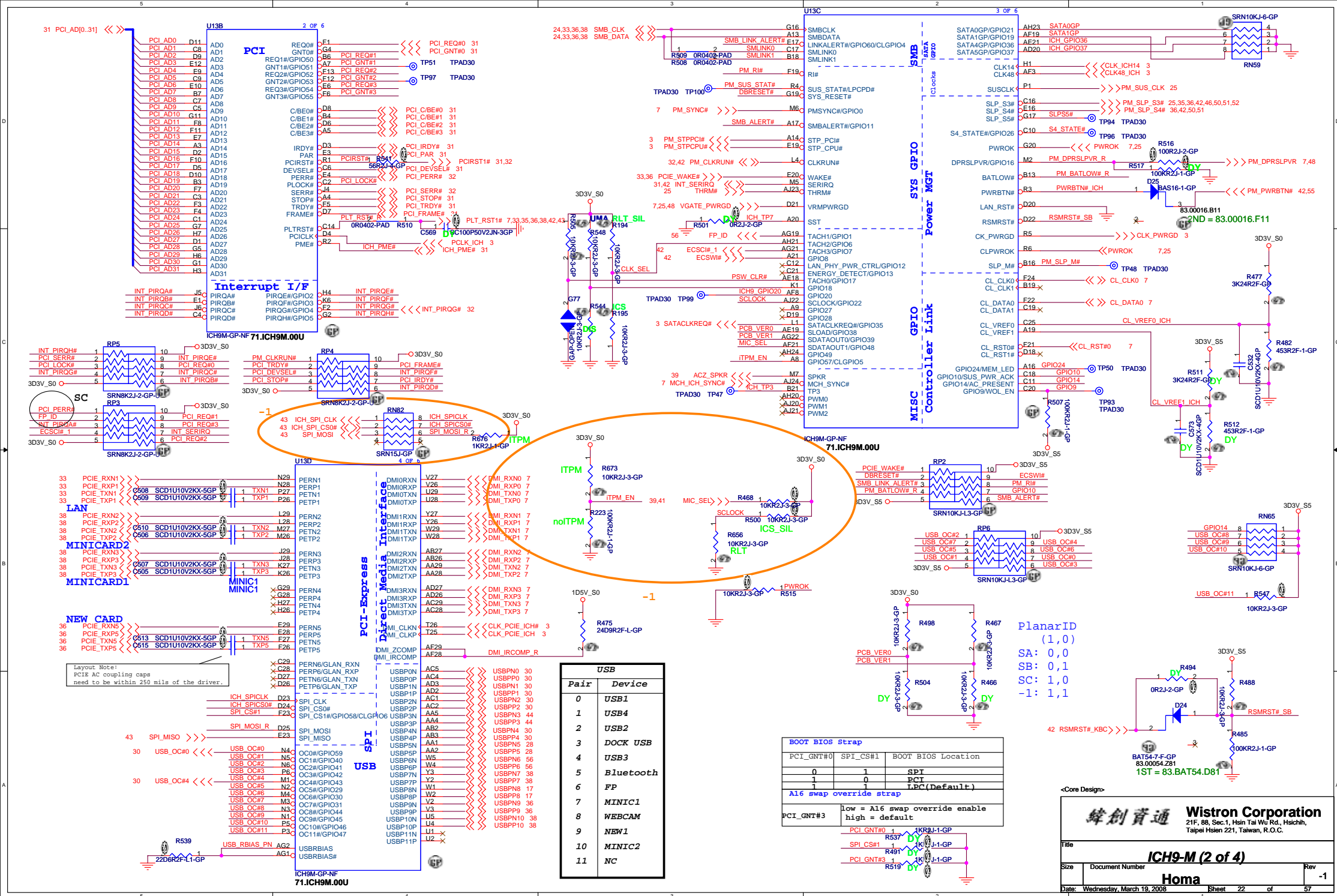


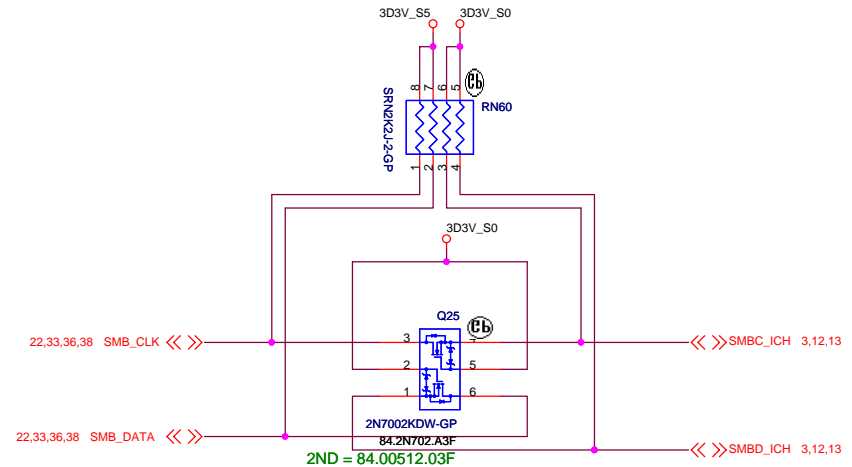
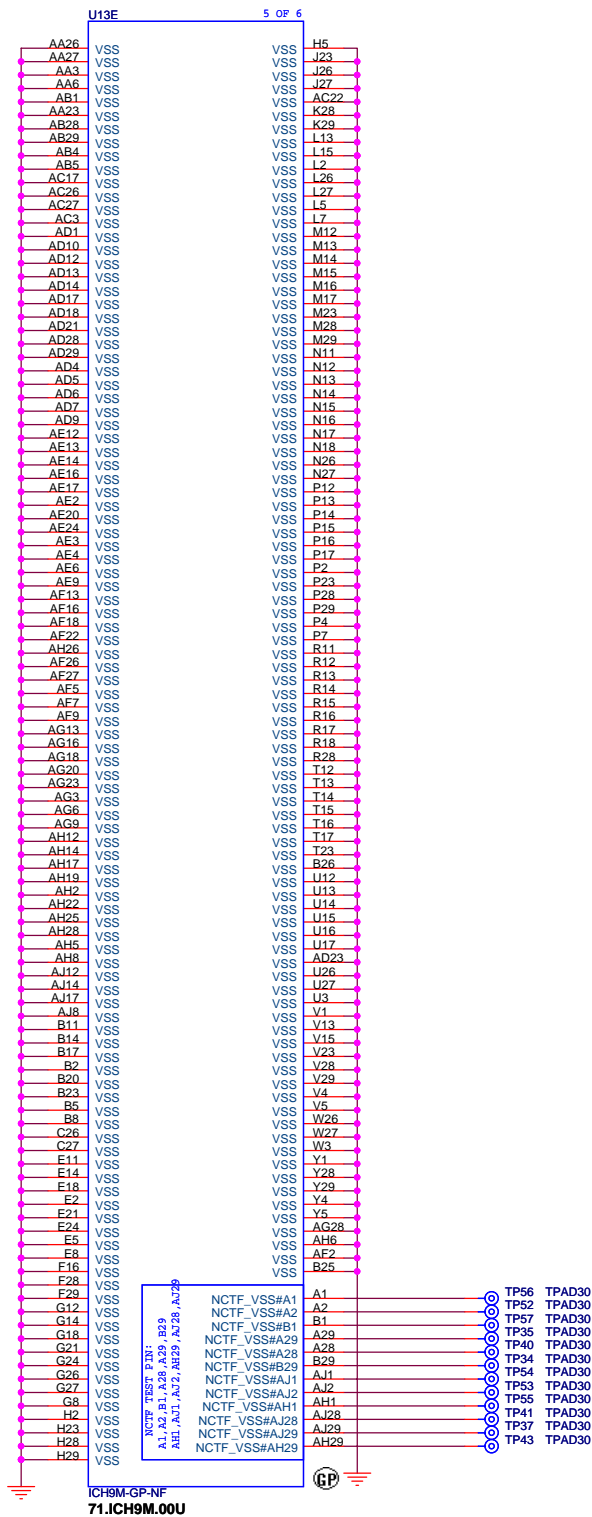
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-1

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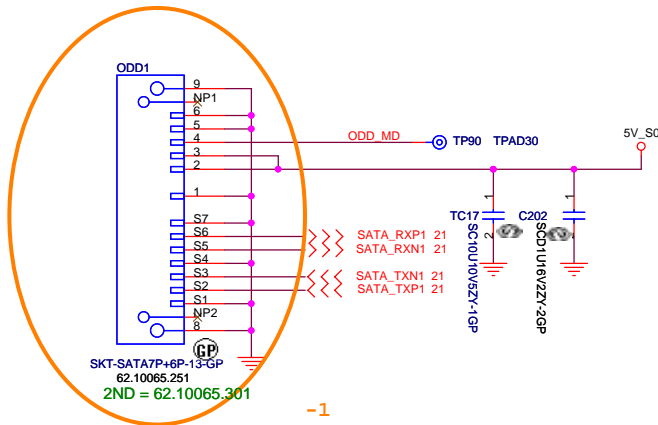




Q13 & Q14 connect SMLINK and SMBUS in S) for SMBUS 2.0 compliance

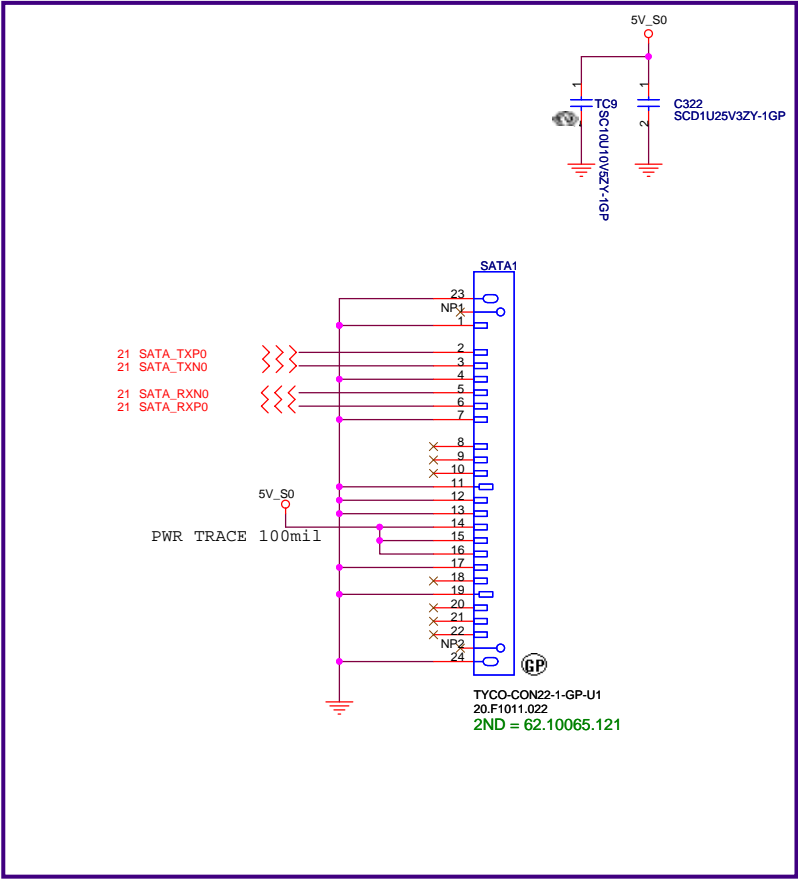
SMBUS

ODD Connector



<Core Design>

SATA Connector



[illegible]

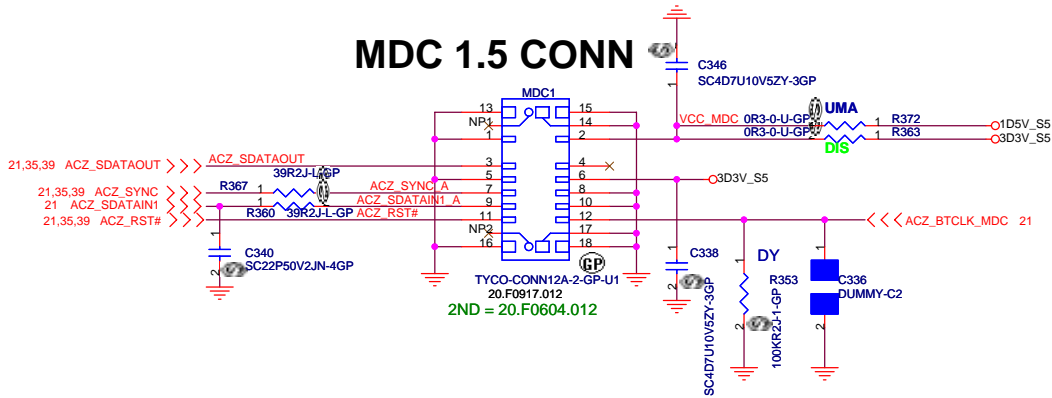
ACES-CON4-1-GP-U1
BLUE1
20.D0197.104
2ND = 20.F0984.004

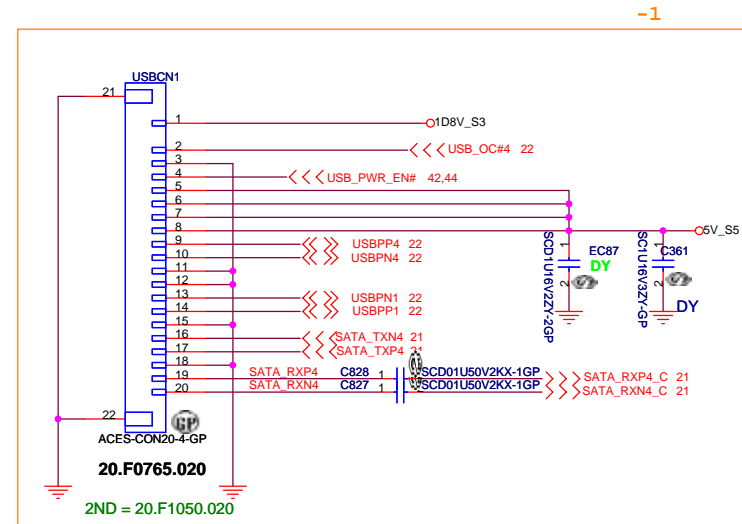
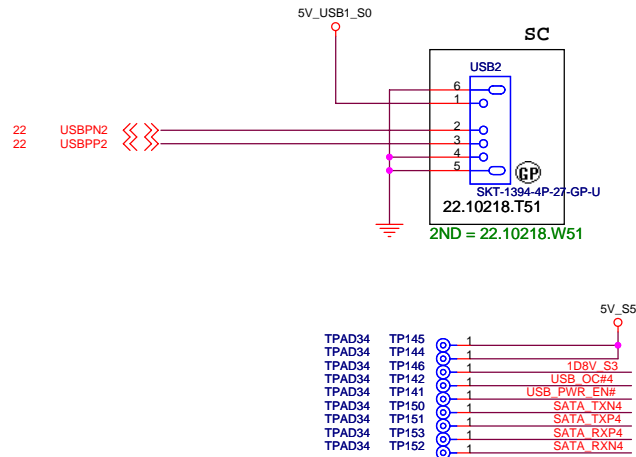
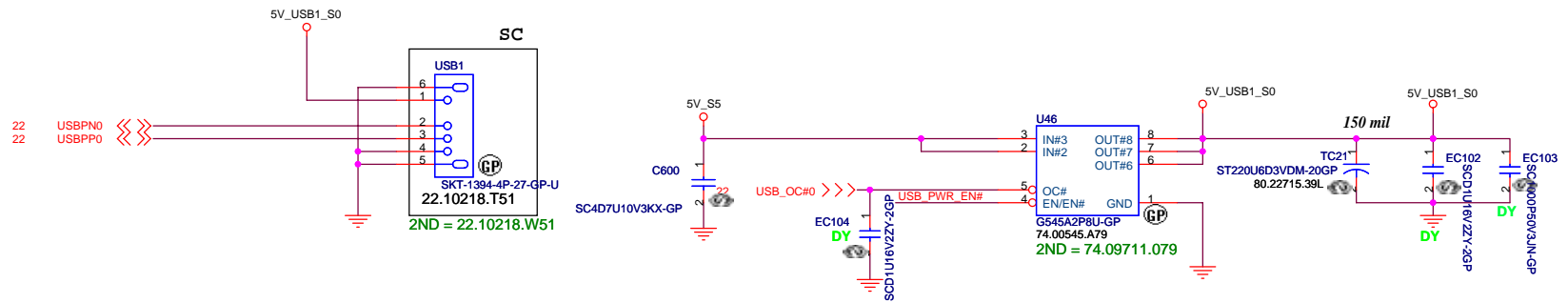
3D3V_BT_S0

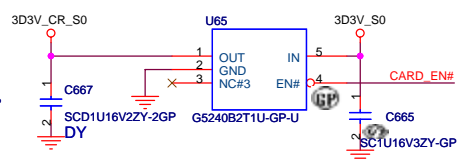
USBPNS 22
USBPPS 22

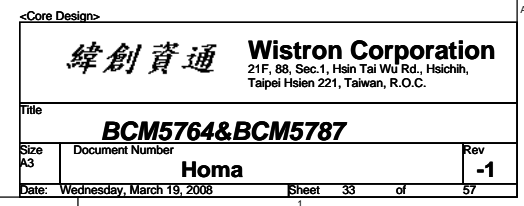
3D3V_BT_S0 1 TP139 TPAD34

MDC 1.5 CONN





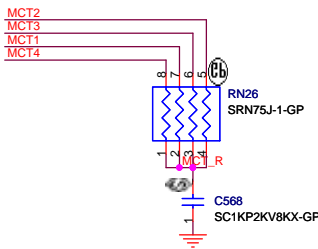
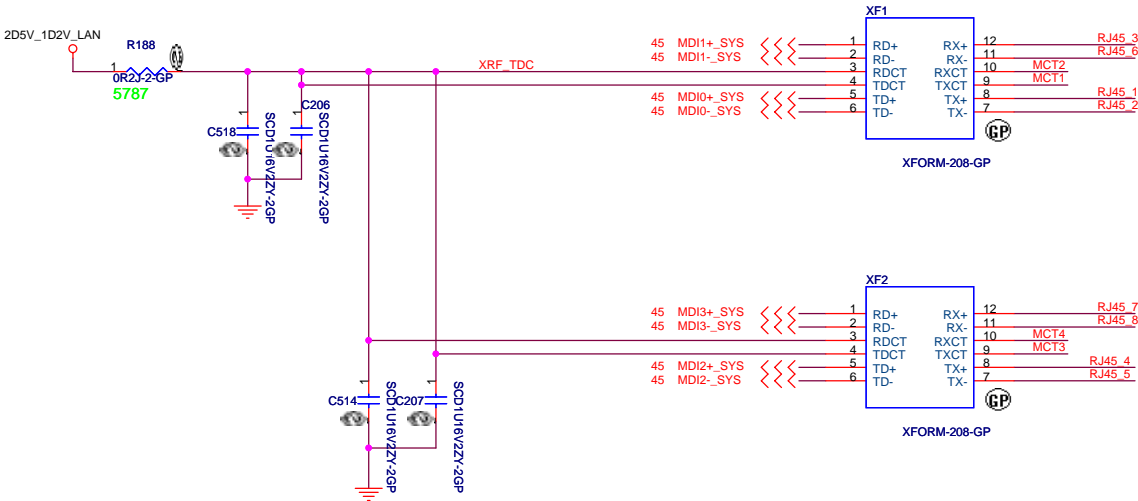




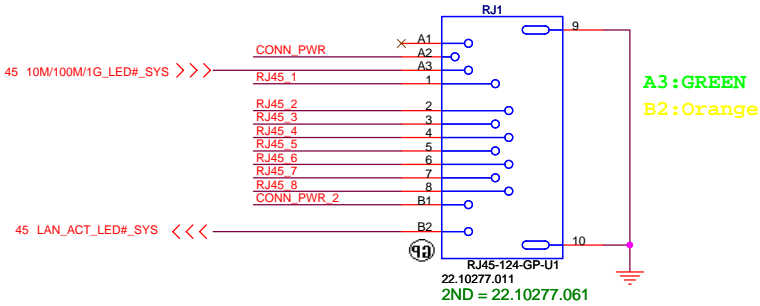
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector

GIGA Lan Transformer

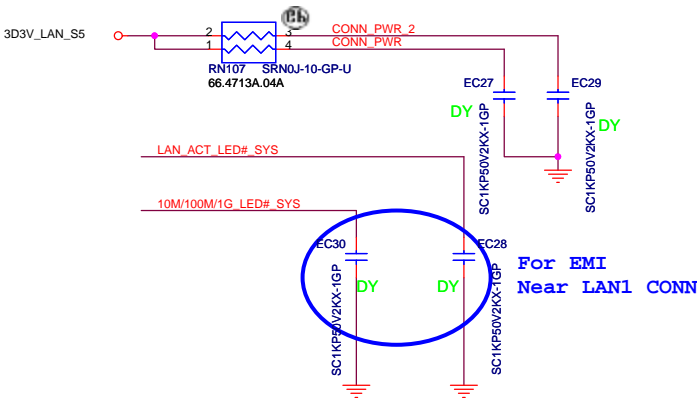


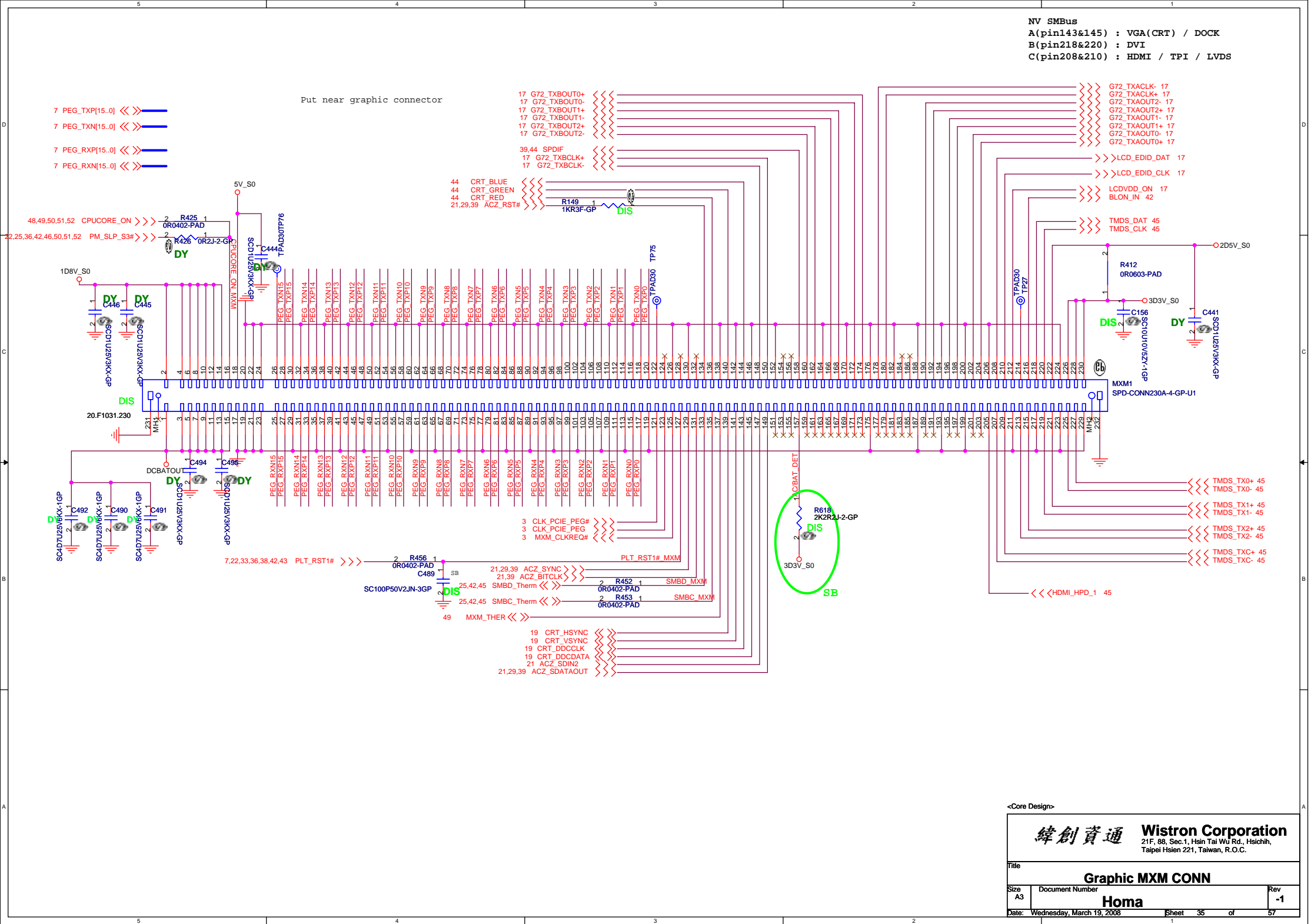
LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

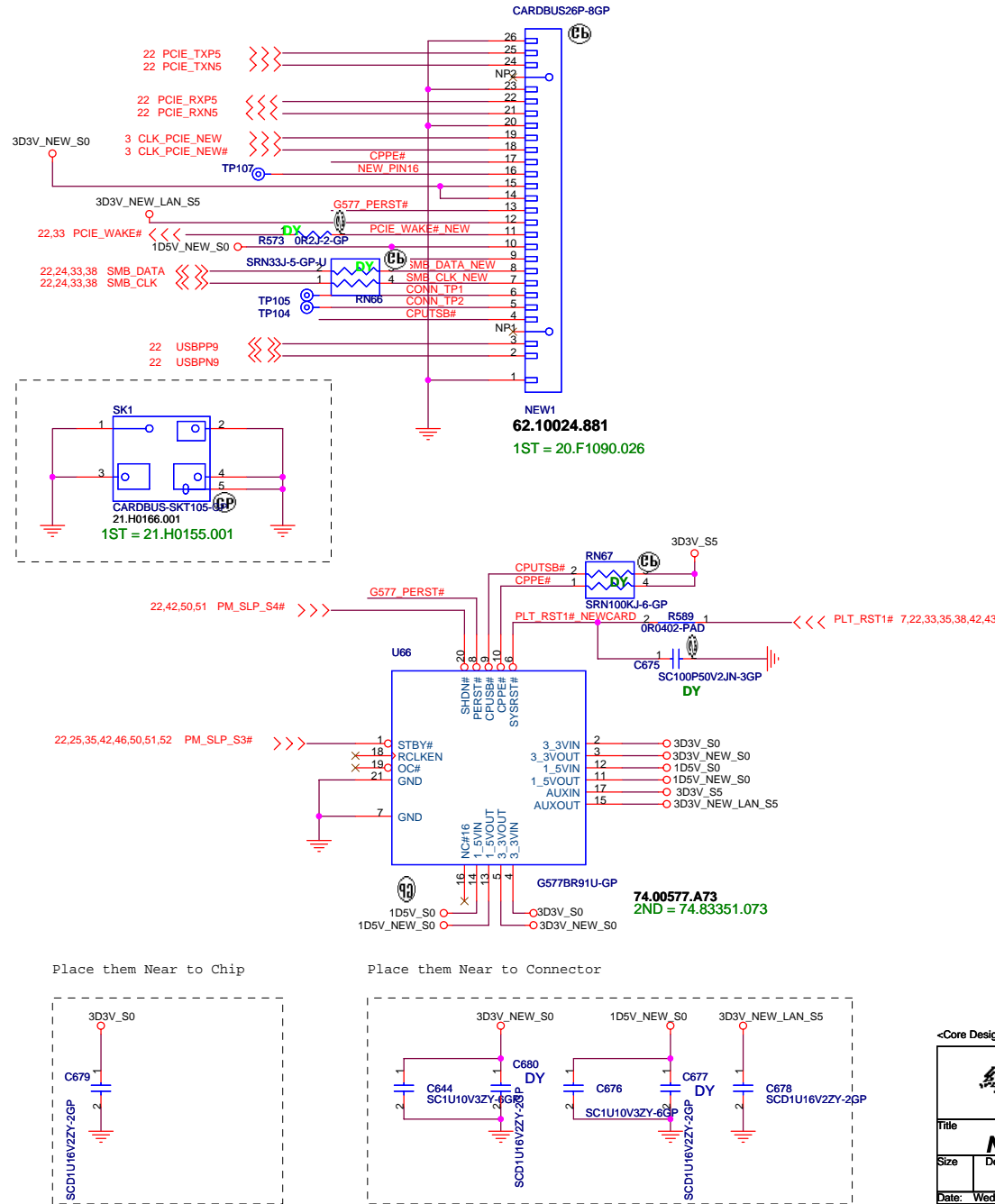
LAN Data: Yellow(B2), when LAN is transferring data.





NEWCARD Connector

Reserve the symbol
for bottom side
connector



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Title NEW CARD		
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PCMCIA Socket

Cardbus I/F

CBB_D[15..0] << >> CBB_D[15..0] 31
CBB_A[25..0] << >> CBB_A[25..0] 31

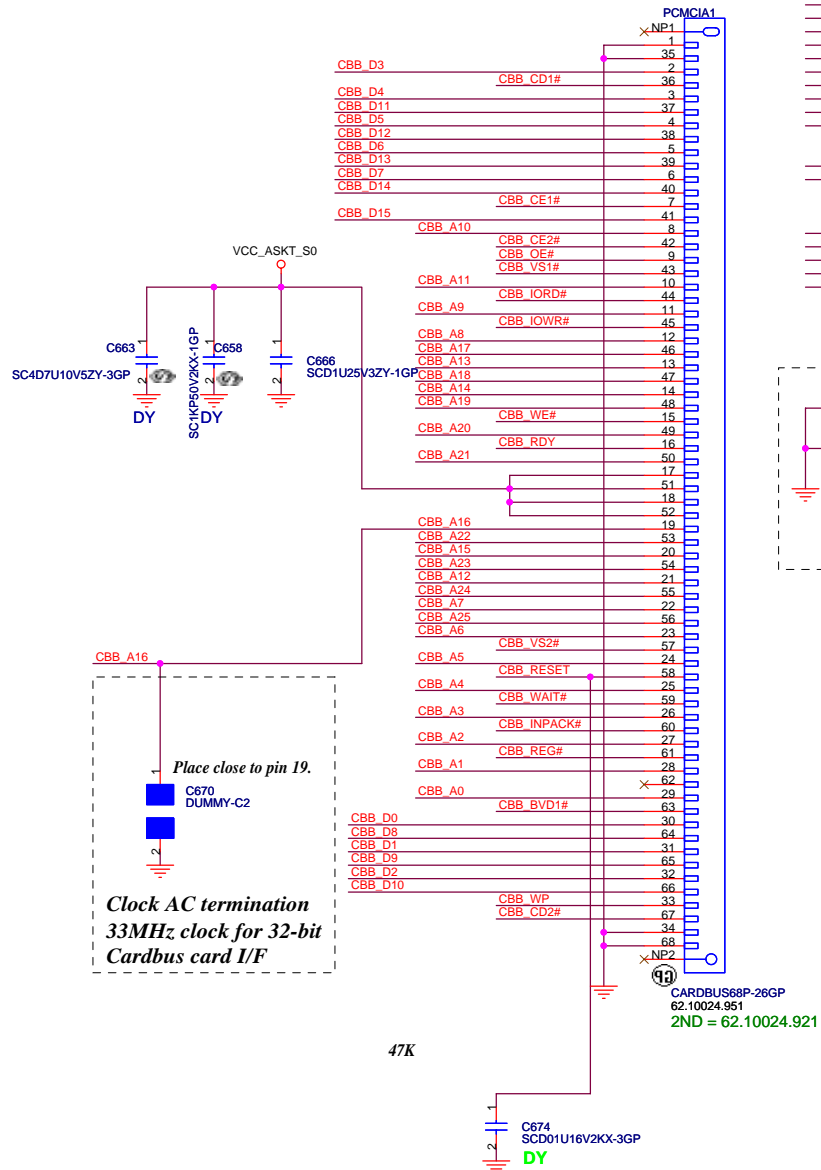
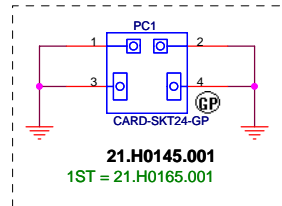
```

—  CBB_IORD# 31
—  CBB_IOWR# 31
—  CBB_OE# 31
—  CBB_WE# 31
—  CBB_REG# 31
—  CBB_RDY 31
—  CBB_WP 31
—  CBB_RESET 31
—  CBB_WAIT# 31
—  CBB_INPACK# 31

```

—	⋈	CBB_CE1#	31
—	⋈	CBB_CE2#	31

—>>> CBB_CD1# 32
—>>> CBB_CD2# 32
—>>> CBB_VS1# 32
—>>> CBB_VS2# 32
—>>> CBB_BVD1# 32



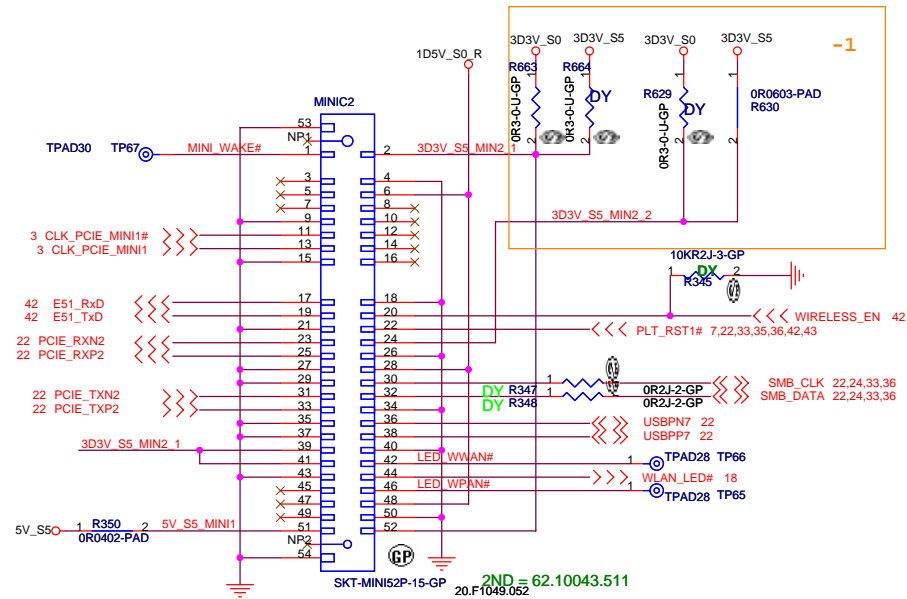
<Core Design>

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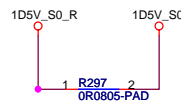
Title	PCMCIA
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Size A3	Document Number Homa	Rev -1
Date: Wednesday, March 19, 2008	Sheet 37 of 57	

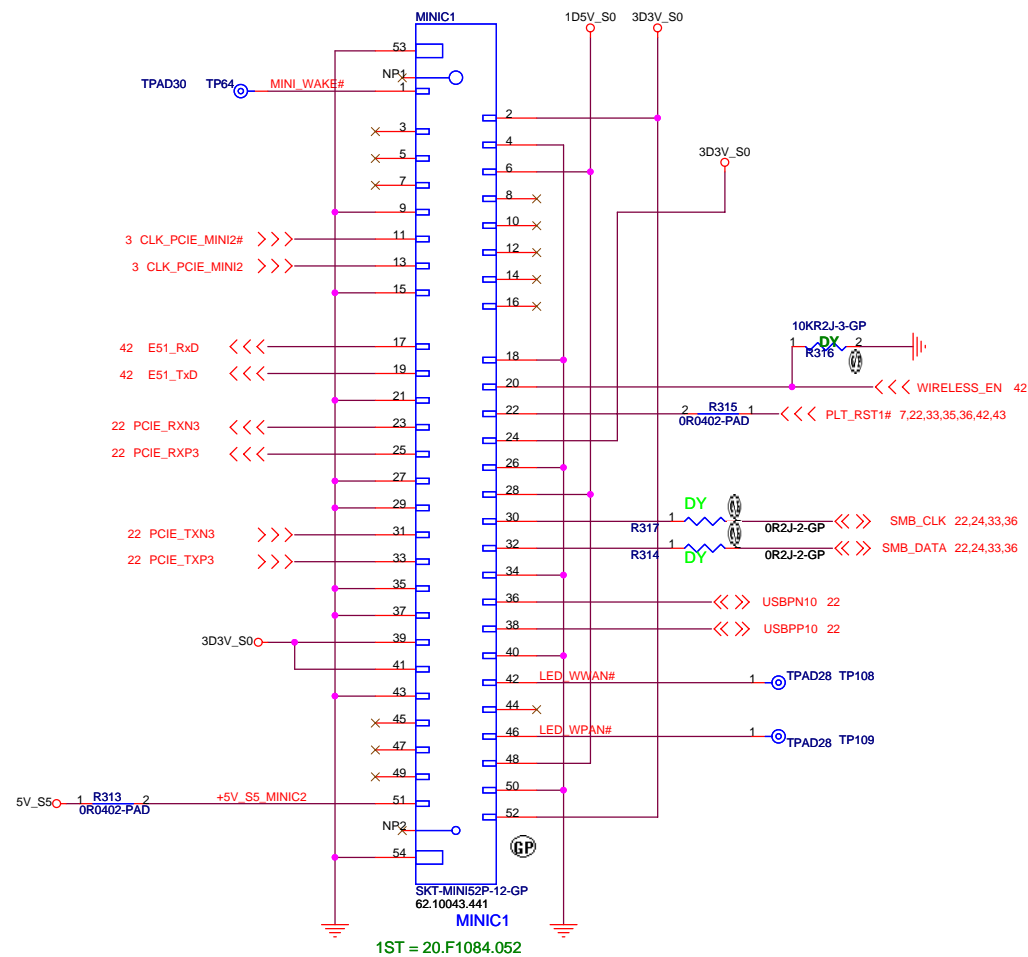
Mini Card Connector(WLAN)



Vo(cal.)=1.5024V OCP>3.2A

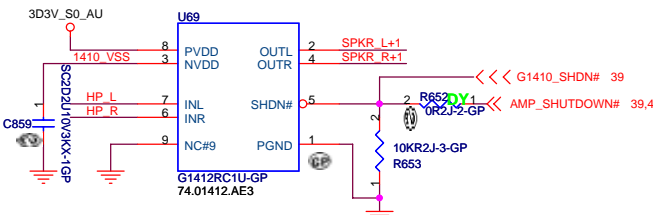
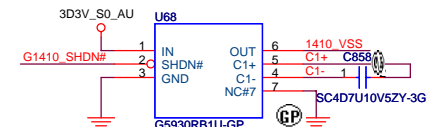
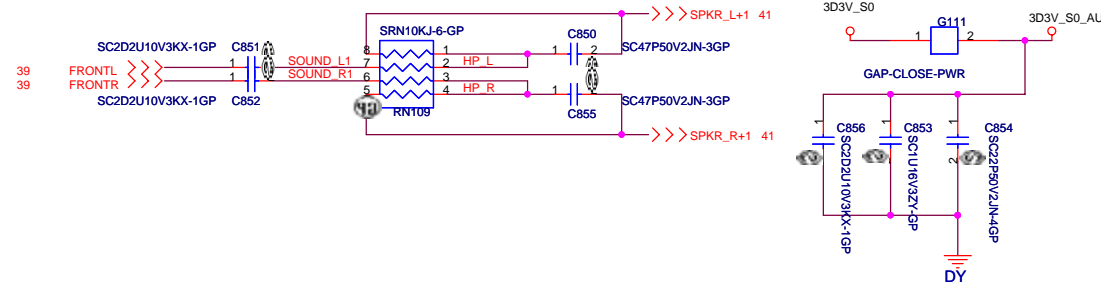
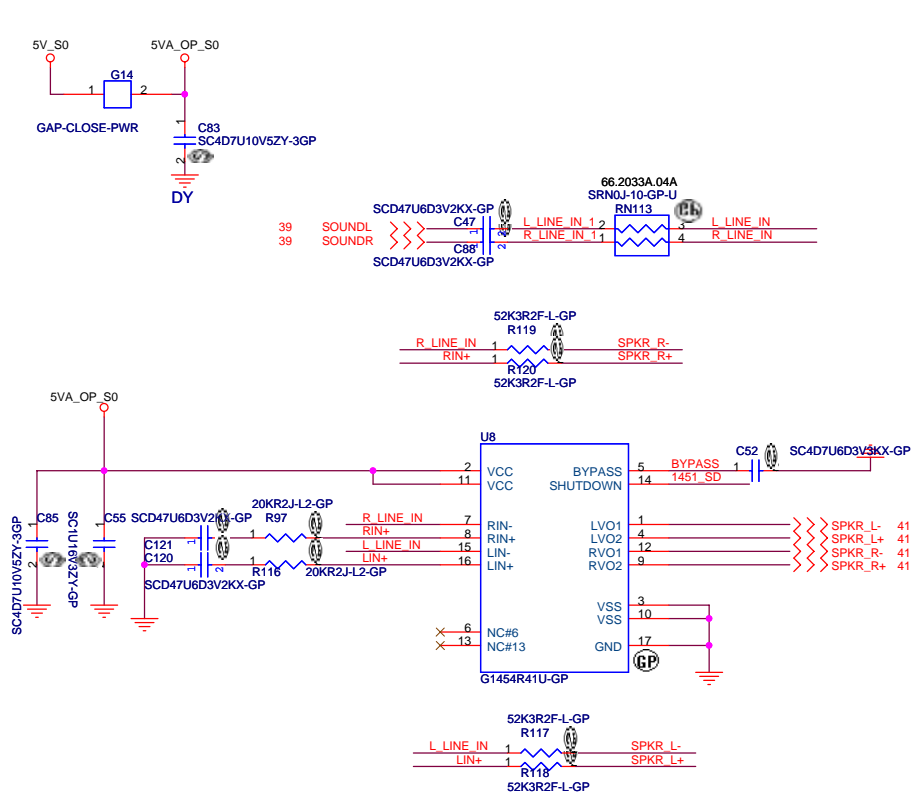


Mini Card Connector

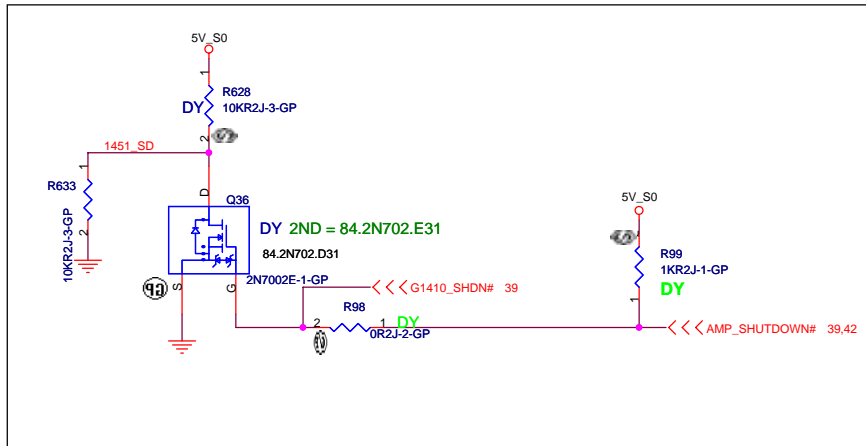


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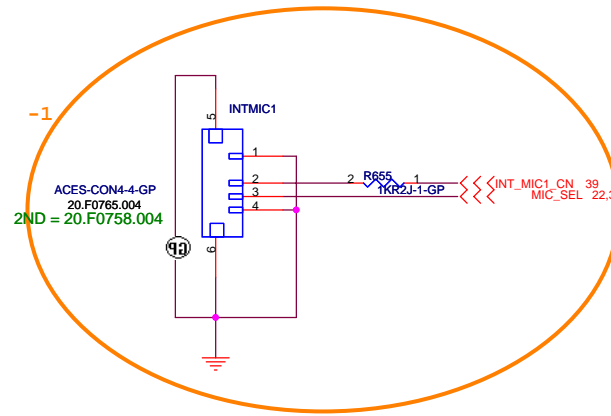
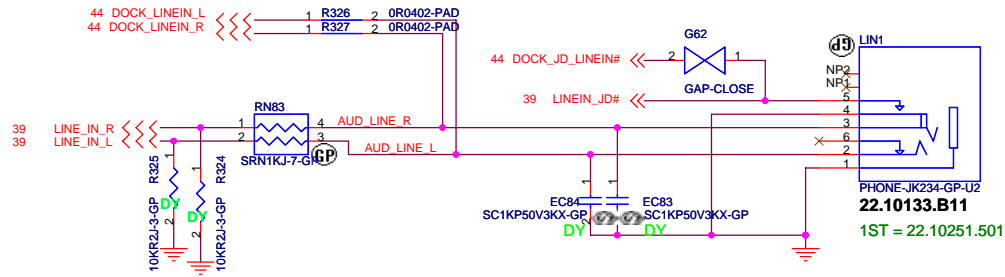
AUDIO OP AMPLIFIER



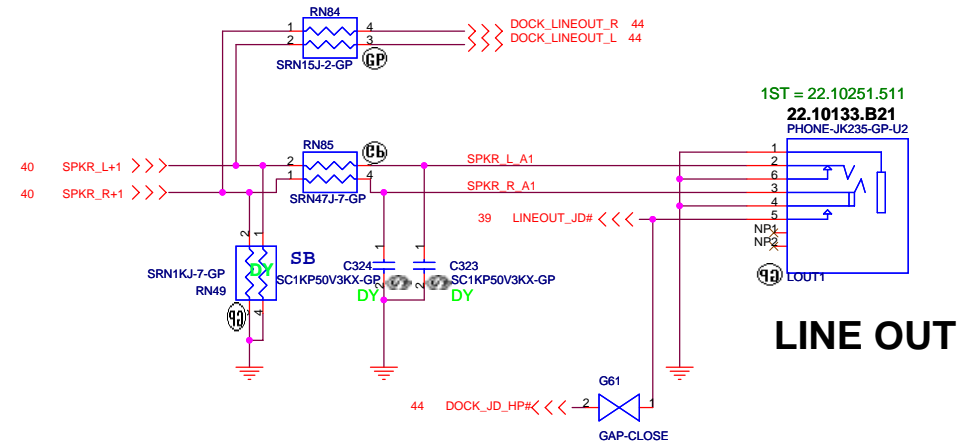
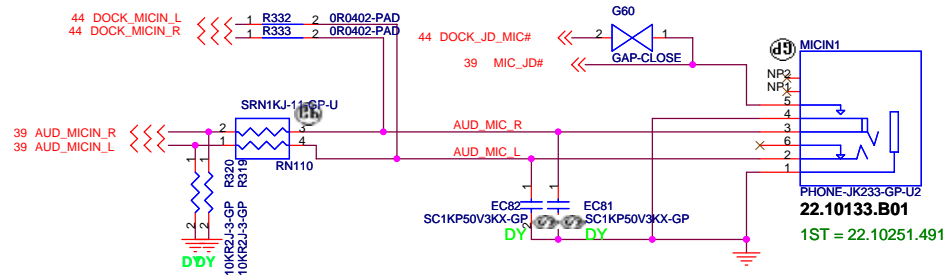
SC



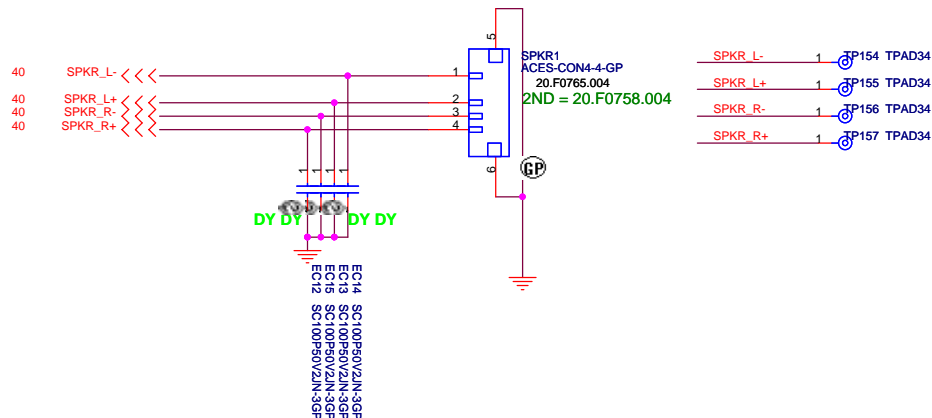
LINE IN



MIC IN



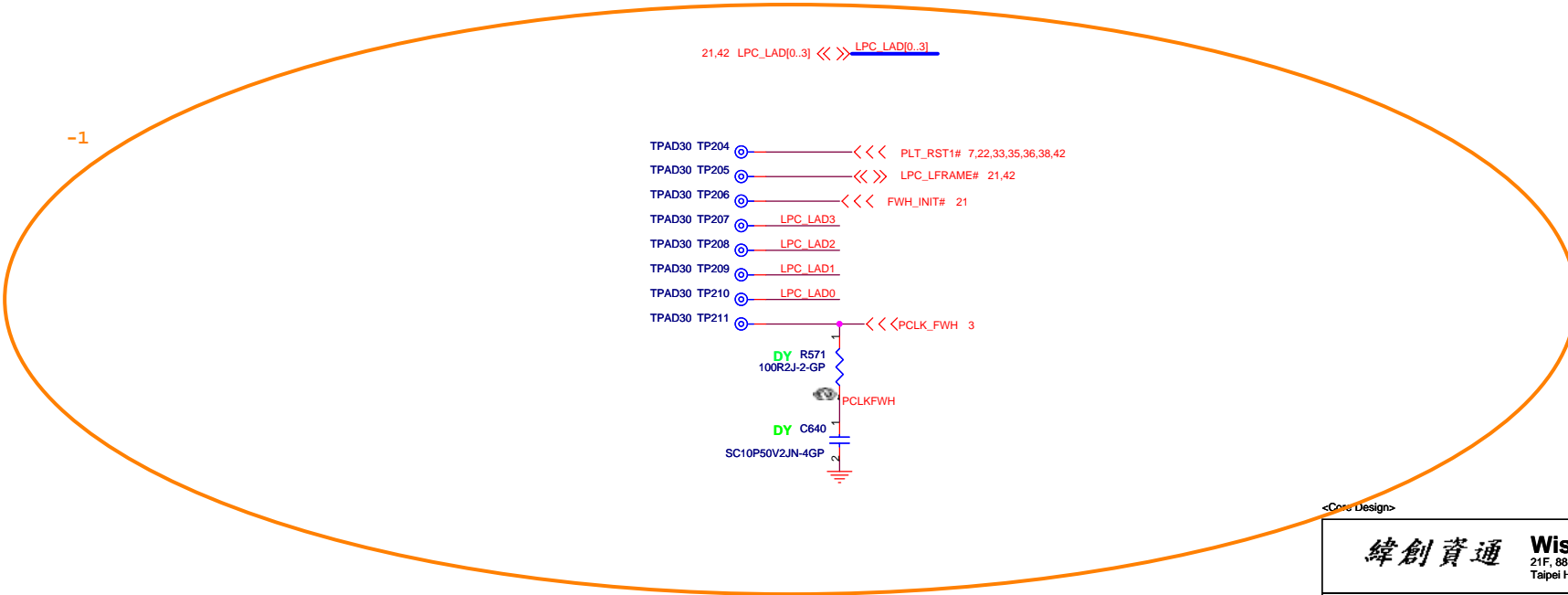
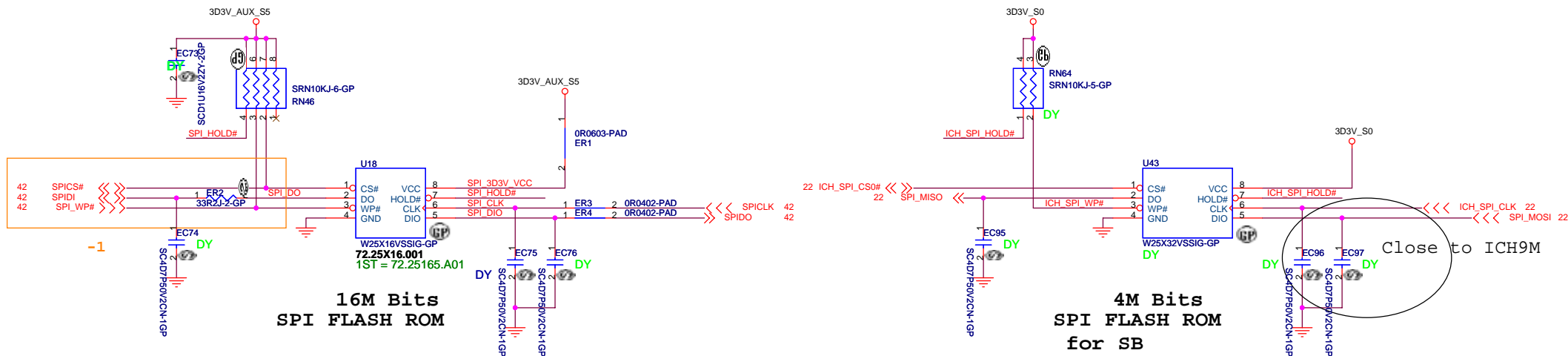
Internal Speaker



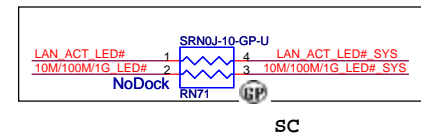
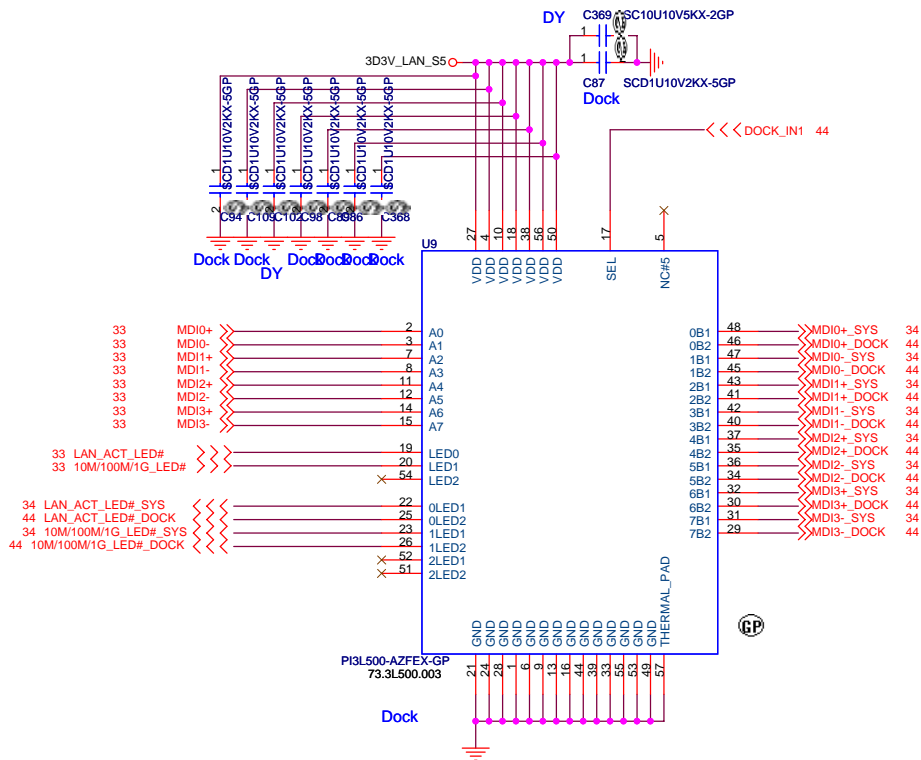
<Core Design>

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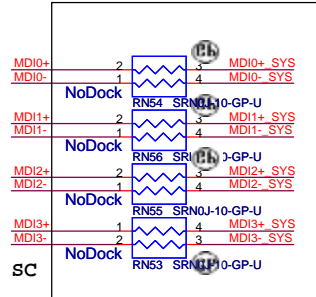
Title			AUDIO JACK
Size	Document Number	Homa	
Date: Wednesday, March 19, 2008	Sheet 41	of 57	Rev -1



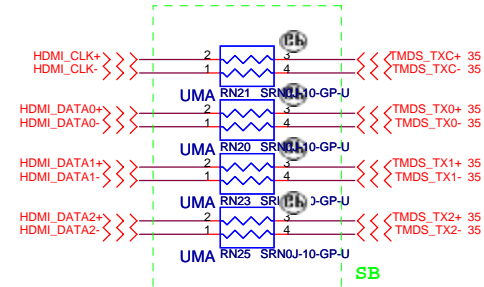
LAN switch



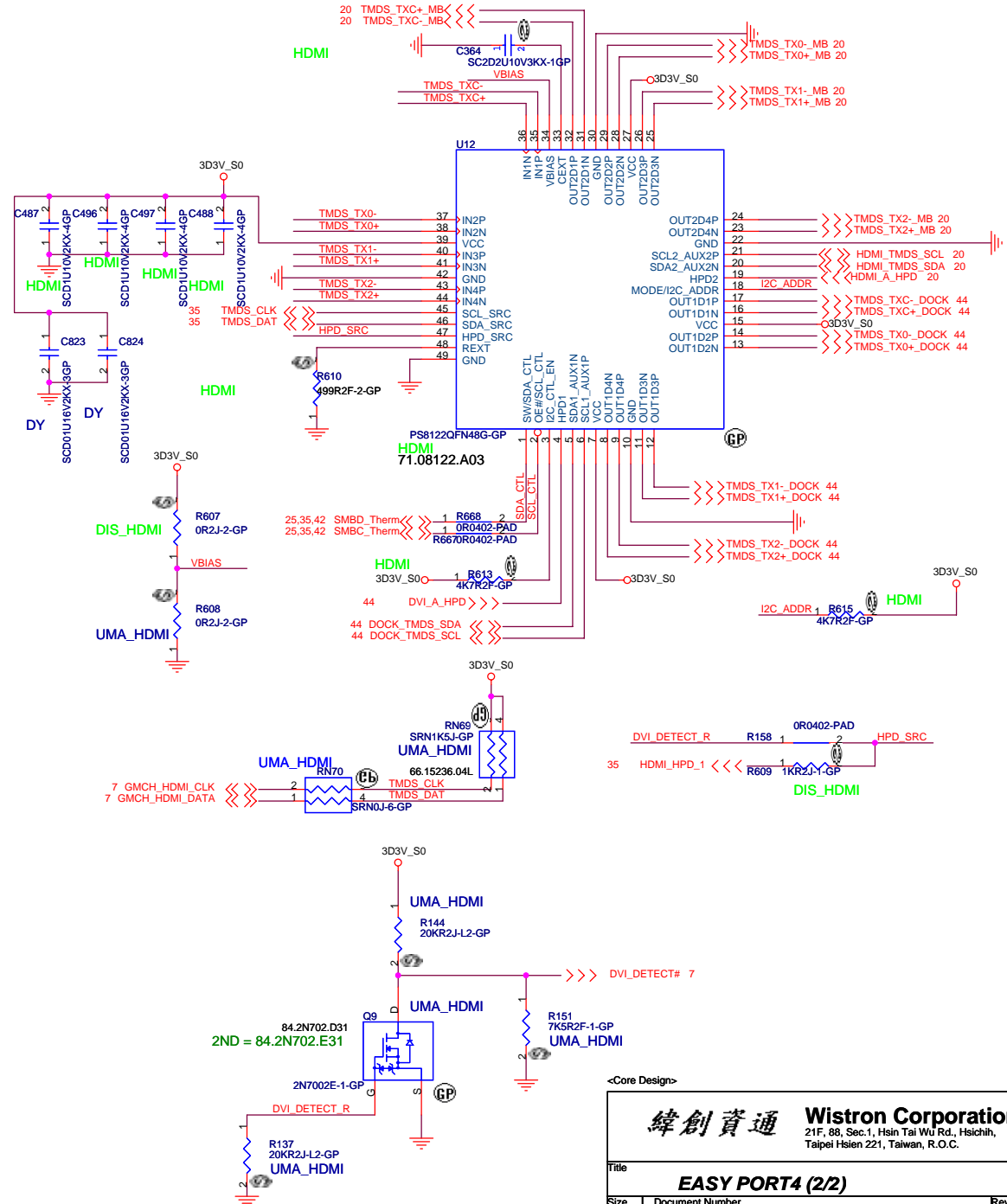
SC



SC



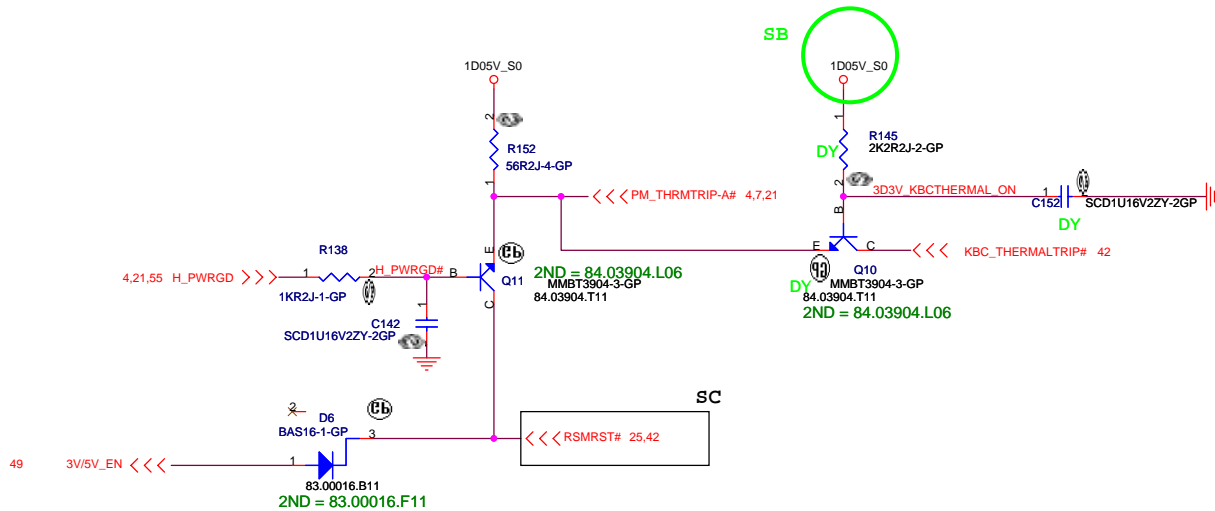
SB



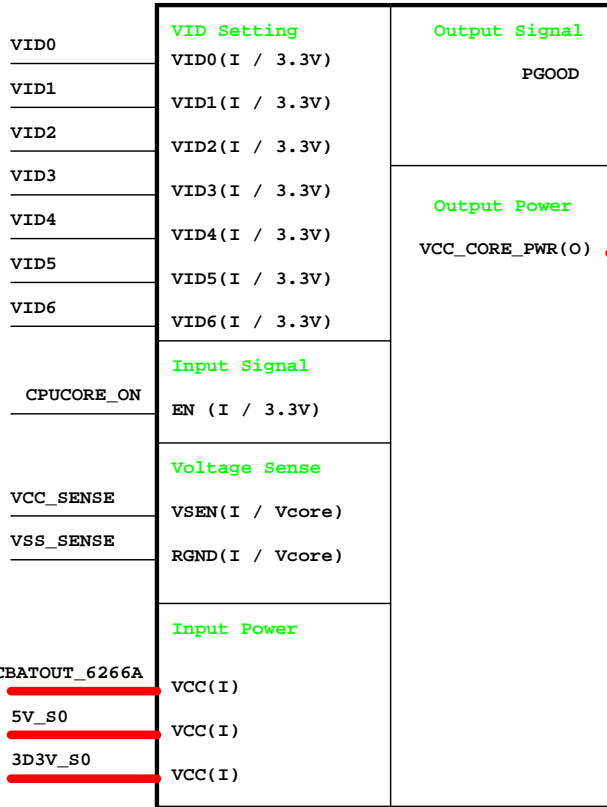
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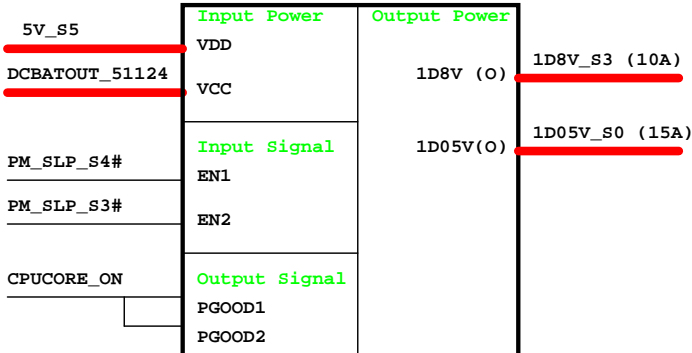
EASY PORT4 (2/2)			
Title	Size A3	Document Number	Rev
		Homa	-1
Date: Wednesday, March 19, 2008	Sheet 45	of	57



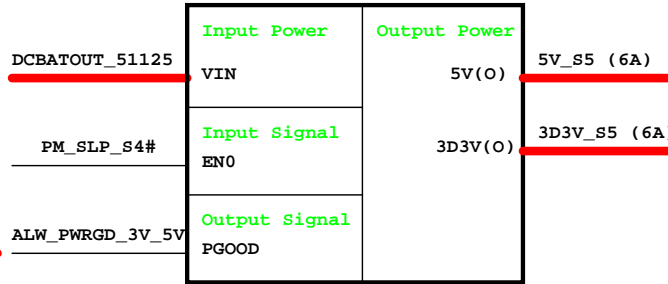
CPU_CORE
ISL6266A



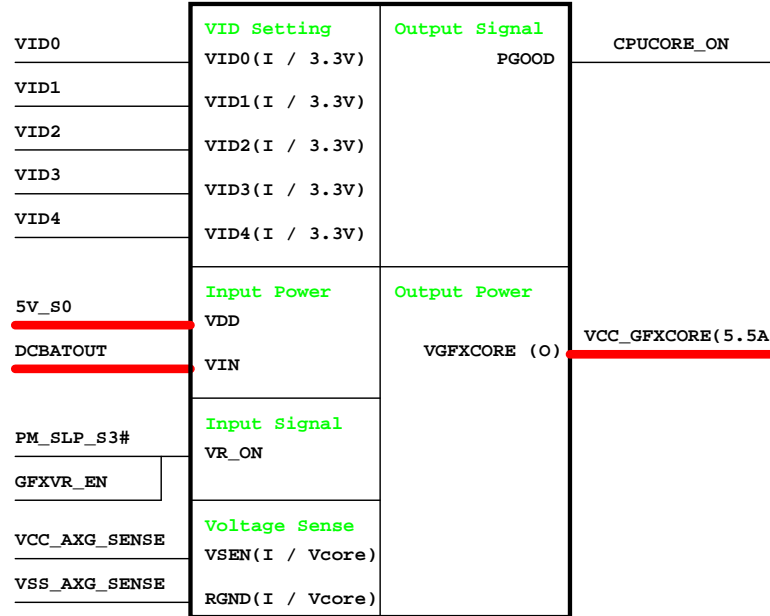
TPS51124
1D8V/1D05V



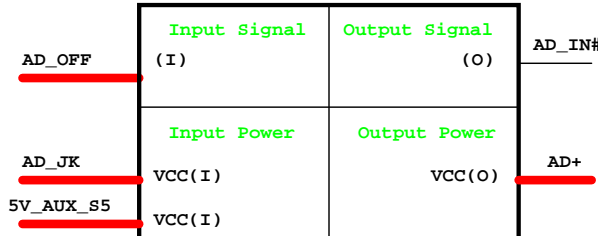
TPS51125
5V/3D3V



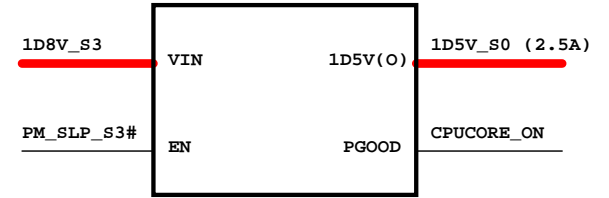
GFX_CORE
ISL6263A



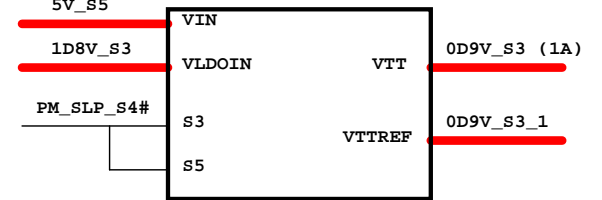
Adapter



RT9018A
1D5V_S0



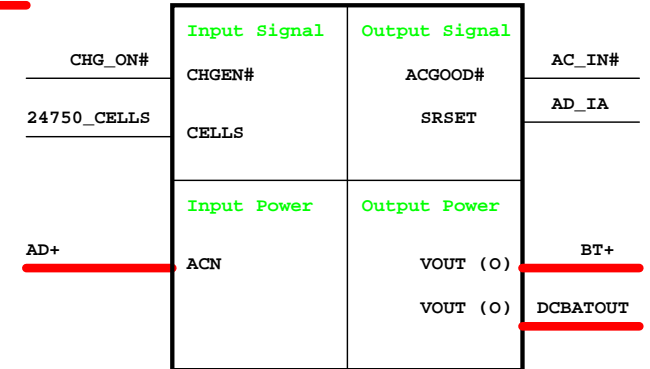
RT9026 0D9V_S0



G9131 2D5V_S0



Charger BQ24750

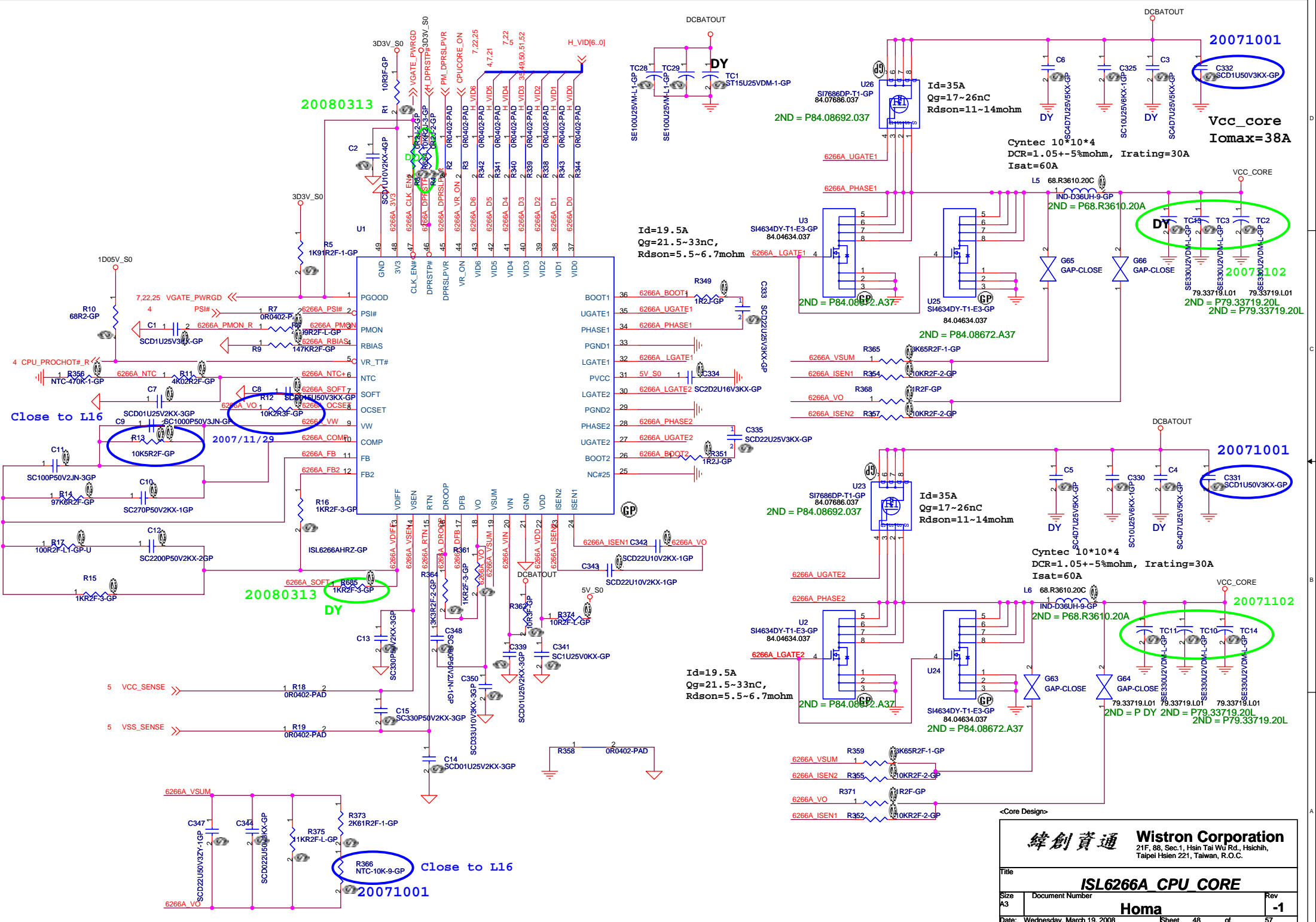


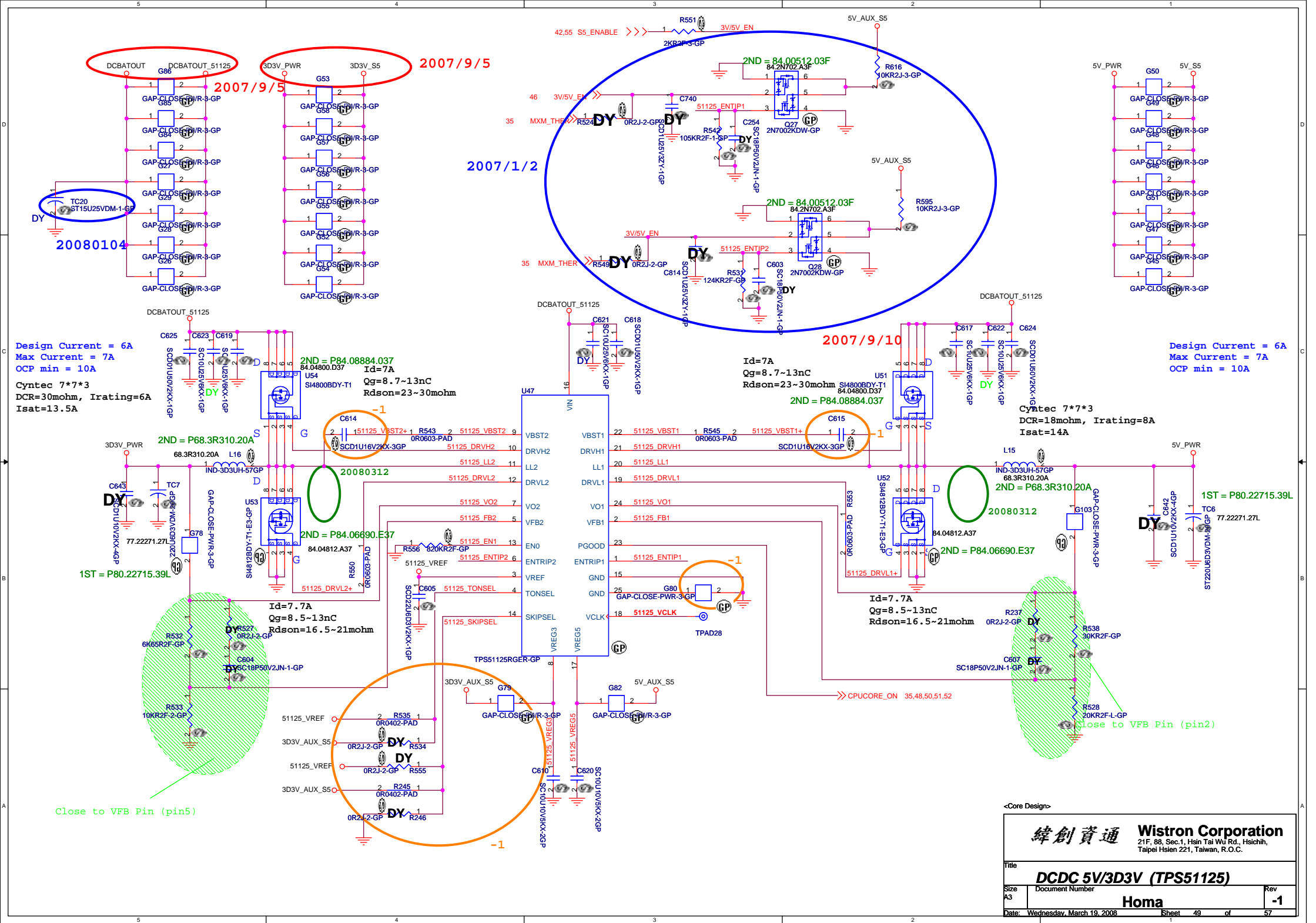
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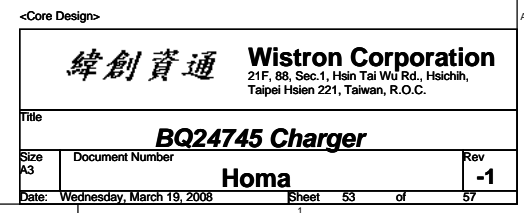
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Title			Power Sequence Logic	
Size B	Document Number		Homa	Rev -1
Date: Wednesday, March 19, 2008	Sheet 47	of 57		

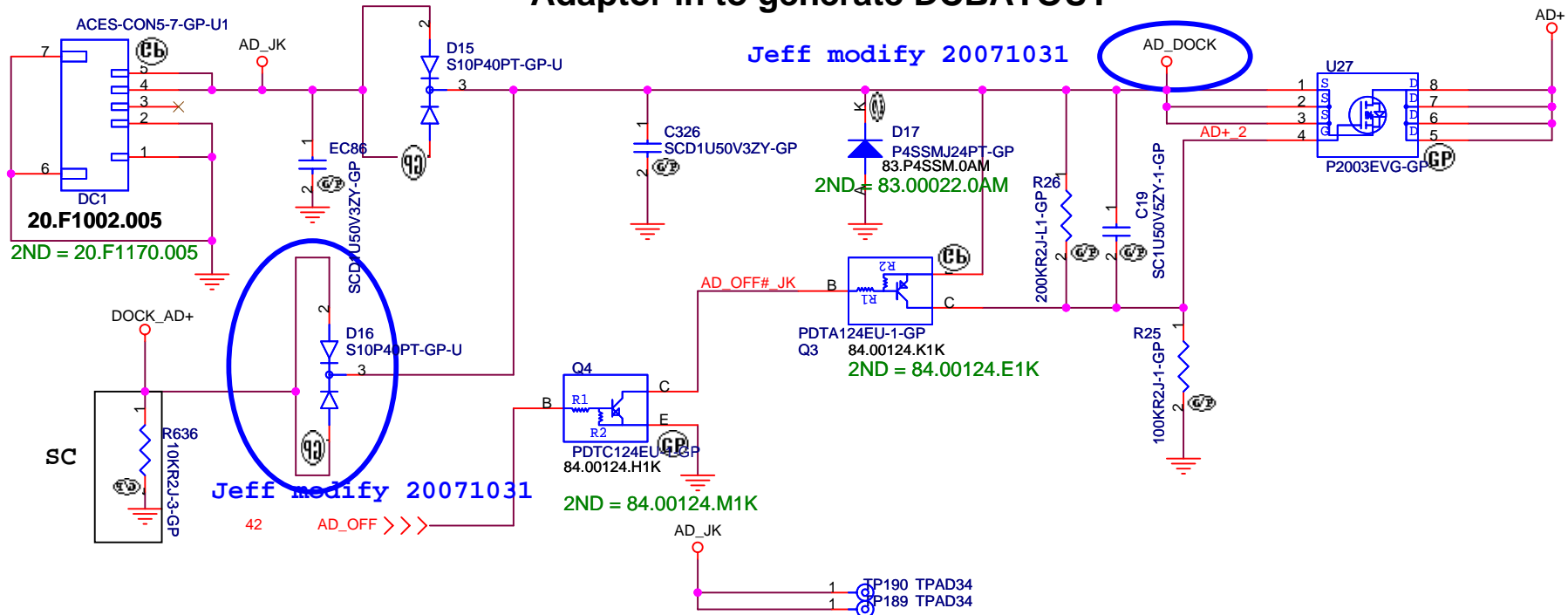




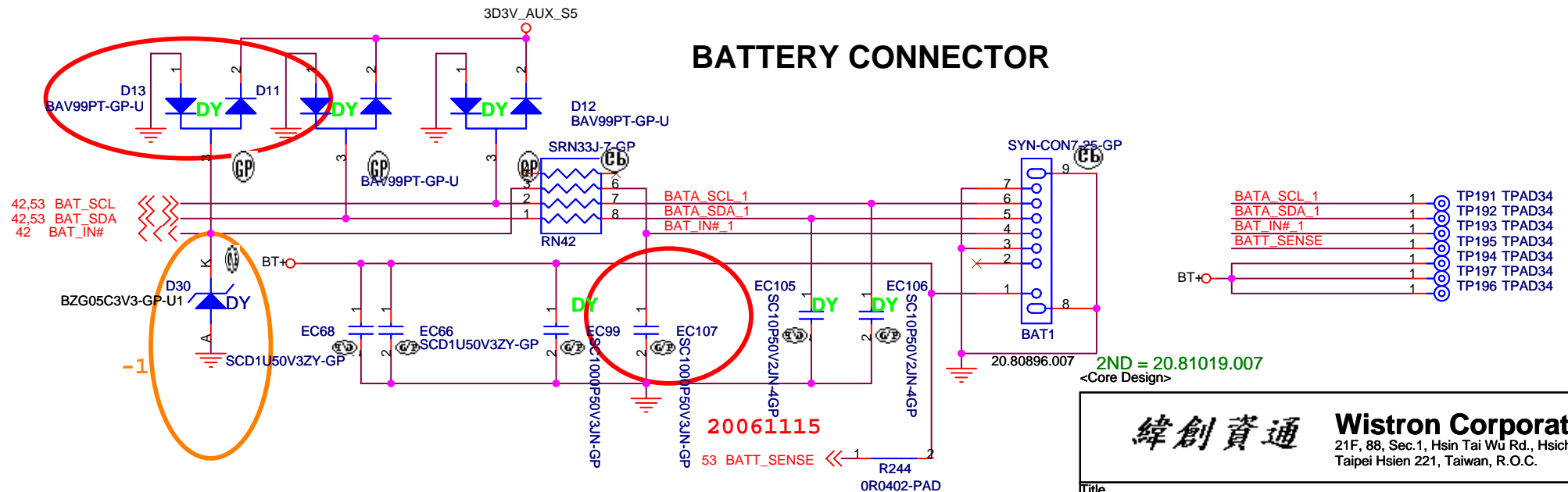


Adaptor in to generate DCBATOUT

Jeff modify 20071031



BATTERY CONNECTOR

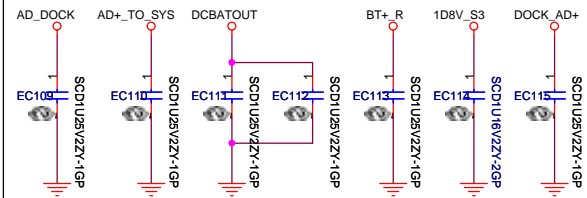





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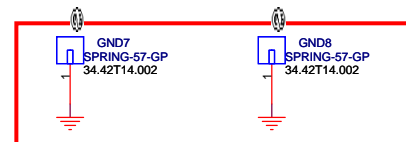
Title				
AD/BATT CONN				
Size	Document Number			Rev
	Homa			-1
Date:	Wednesday, March 19, 2008		Sheet 54 of	57



3D3V_S0		TP110 TPAD30
3D3V_AUX_S5		TP111 TPAD30
3D3V_S5		TP112 TPAD30
5V_S5		TP113 TPAD30
22,42 PM_PWRBTN#		TP114 TPAD30
4,21,46 H_PWRREQ		TP115 TPAD30
42,49 SS_ENABLE		TP116 TPAD30
4,6 H_CPURST#		TP117 TPAD30

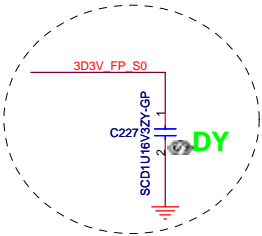
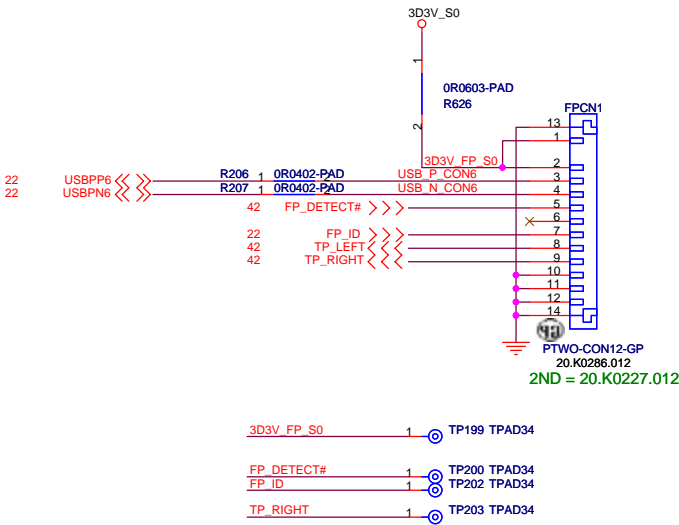
SC

Figure 10 shows four circuit diagrams, each representing a different ground connection point: GND3, GND4, GND5, and GND6. Each diagram illustrates the connection of a component labeled 'SPRING-37-GP-U' to a ground symbol. The measured values for each connection are 34.15F09.001, and the status is 'DIS'.



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Finger printer



For EMI

SA --> SB

- 1.page25,Change Q24 and Q5 Pin_C and Pin_E net, Swap H_THERMDA and H_THERMDC(only close to C95)
- 2.page46,Change R145_Pin1 pull hige power to 1D05V_S0
- 3.page42,Add the Net let link U17_Pin101 and RN45_Pin3
- 4.page16,SWITCHCN1 pin12 connect to 3D3V_AUX_S5 and pin 11 connect to LID_CLOSE#
- 5.page20,HDMI1 change to 62.10078.171
- 6.page44,DOCK1 pin51 connect to CRT_DEC#
- 7.page53,R214 change to connect BQ24745_VREF as charger modify
- 8.page26,change ODD1 to 22.10300.141
- 9.page45,change U12 to PS8122QFN48G-GP and add some components
- 10.page44,Del U5
- 11.page20,Del U11,U42,Q9...
- 12.del G1-G8
- 13.page45,R614 changed to "DOCK_DT1#" and U12 output port1 and port2 swap,RN68 pin1&2 change to KBC SMBUS, RN69 pin3&4 change to connect"3D3V_S0",R615 change to 4K7R2F-GP
- 14.page49,change Q27&Q28 to 2N7002SPT ,add R595 R616
- 15.page48,change R12 to 10K2R3F-GP ,R13 to 16K5R2F-1-GP
- 16.page51,R578 change to 22K1R3-GP
- 17.page52,R257 change to 2K87R2F-1-GP ,C259 change to SCD033U50V
- 18.page40,change U8 to G1454R41U-GP
- 19.page42,Del R29 R27 C20 EC5
- 20.page41,LID1 change to INTMIC1 and connect to "MIC_L_CN"&"MIC_R_CN"
- 21.page39,add R619 C815 R621 R620 C816 C817
- 22.page38,Del C355 C320
- 23.page56,Del F4 addR626
- 24.page3,R204 change to connect"3D3V_CLKPLL_S0"
- 25.page52,add R622-R625
- 26.page44,add C818-C822 and L19 L20 L21
- 27.page35,Del TP77-TP82 TP84 TP86 TP87 TP24 TP25 TP26 TP28,add R618 pull up to 3D3V_S0
- 28.page25,add R617 Q35 del R115
- 29.page30,change C600 to 4.7U10V
- 30.page45, swap U12 output port1&pot2
- 31.page48~52, change power GAPs to close GAPs
- 32.page49,L15 change to 1ND-3D3UH by power modify
- 33.page16,add R627 EC108
- 34.page45,add C823 C824 and R144 R151 Q9 R137

<Core Design>

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